DIY Direct Digital Synthesis (DDS) with TTL ICs

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1 Introduction

This project was one of several activities I engaged in during the Covid Summer of 2020. I had thought about building a simple Direct Digital Synthesis (DDS) circuit in the past but never found the time to do it. Now the virus provided a window of opportunity for these types of of projects.

What is Direct Digital Synthesis? DDS is one of the foundations of Software Defined Radios (SDR). The signals output by SDR radios are universally created using DDS techniques. In SDR radios the DDS generates a simple Sine wave or a Sine wave modulated by a voice or data signal. This paper documents the design and construction of a DDS circuit constructed with TTL (74LS series) digital components.

1.1 Mapping the Sine function to the digital domain

It is necessary to provide a mapping between the Sine function Figure 1 and the binary number system used in the DDS. The Sine function's domain (input) is the range $[0, 2\pi]$ radians, and its domain (output) is $[1-, 1]$. The Sine function is stored a ROM component where binary integers are stored that approximate the Sine function. Sine function's range values are translated into address values that are used to look up binary values. This is a translation between continuous real numbers and discrete numbers. The binary values stored in the ROM can be computed using this formula:

$$rom(\theta) = \left\lceil sin\left(\frac{\theta 2\pi}{2^N}\right) + 1 \times \frac{2^{n-1}}{2} \right\rceil \tag{1}$$

Where: n is the ROM's word size in bits,
N is the ROM's address bus size in bits,
and θ is the Sine function angle, $\theta \in \{0, 1, \ldots, 2^N - 1\}$.
Figure 2 is a plot of the contents of the Sine ROM. Note the ranges of the abscissa [0,65535] and the ordinate [-1,1] axes.

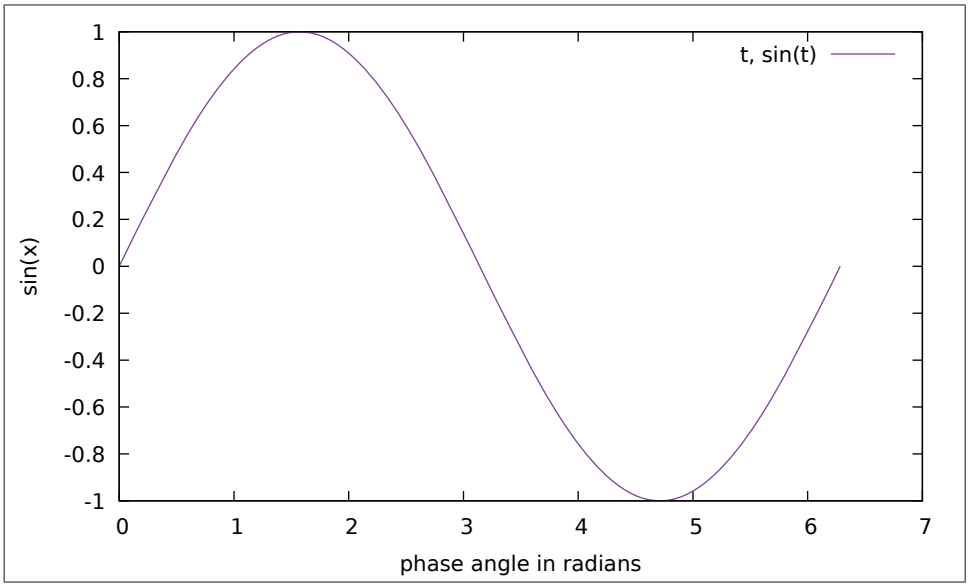


Figure 1: Sine Function

2 System Design

Figure 3 is a top level block diagram of the DDS project. The DDS system contains three major components: a control section, phase accumulator, and output section. The control section acts as the interface between the outside and the DDS. The phase accumulator generates a series of binary numbers (signal phase values) 100,000 times per second. The phase values are used to step through the sine function ROM. Finally, the output section converts each signal phase value to a binary number approximating the sine function's amplitude for that phase, and converts the binary amplititude value to an analog output signal.

The frequency resolution of a DDS system is given by:

$$\Delta f = \frac{f_{clk}}{2^N} \tag{2}$$

Where N is the phase accumulator's size in bits, and f_{dds} is the DDS clock frequency.

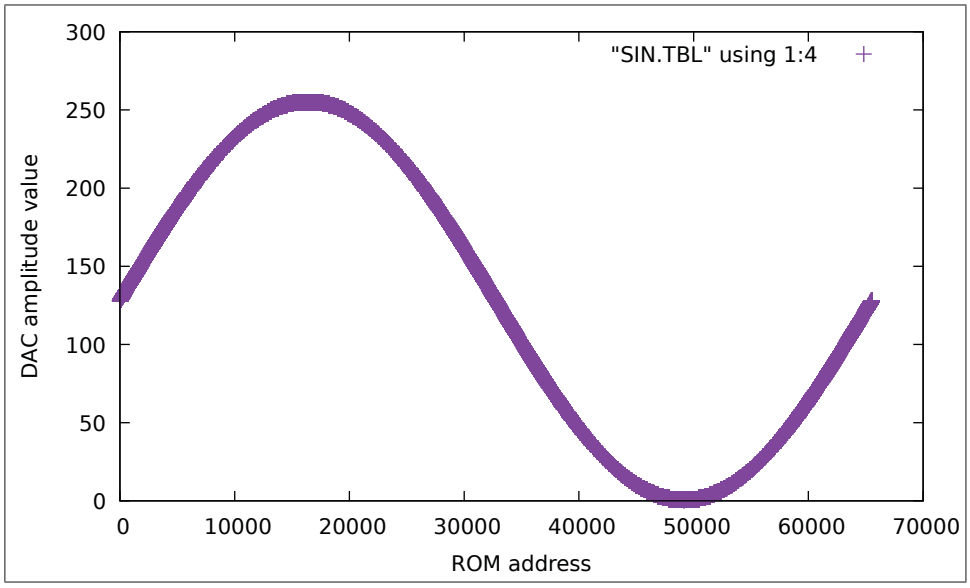


Figure 2: Sin ROM

The tuning word value is calculated using this formula:

$$t_w = \left\lfloor \frac{f}{\Delta f} \right\rfloor \tag{3}$$

Where f is the desired output frequency.

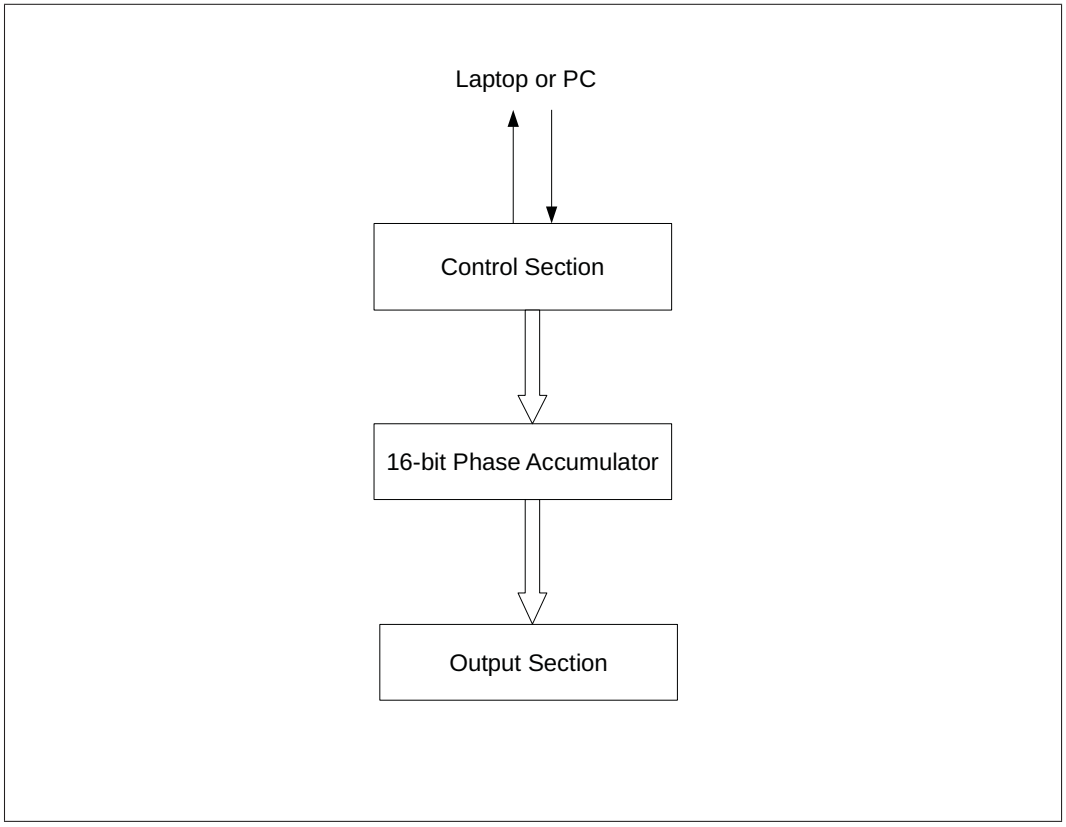


Figure 3: Top Level Block Diagram

2.1 Control section

Figure 4 shows the organization of the control section. The control section provides an intelligent interface between the DDS and an external computer. The external computer can command the operating frequency by sending command strings of ASCII characters to the DDS. The desired output frequency is converted to a 16 bit binary value that is stored in a 16 tuning, register implemented by two 74LS164 Serial-in-Parallel-Out (SIPO) ICs. The firmware running in the PIC micro-controller (PIC16F628A-IP) and several support utilities are available on github at `https://github.com/kb2ghz/DDS-SW`. In addition, the control section provides a 2-phase 100 kHz clock that is used to control the timing of the phase-accumulator. The 2-phase clock is implemented by routing the micro-controller's 10 MHz clock through two 74LS90 ICs configured as divide by 10 counters. Figure 6 shows the 100 kHz clock signals.

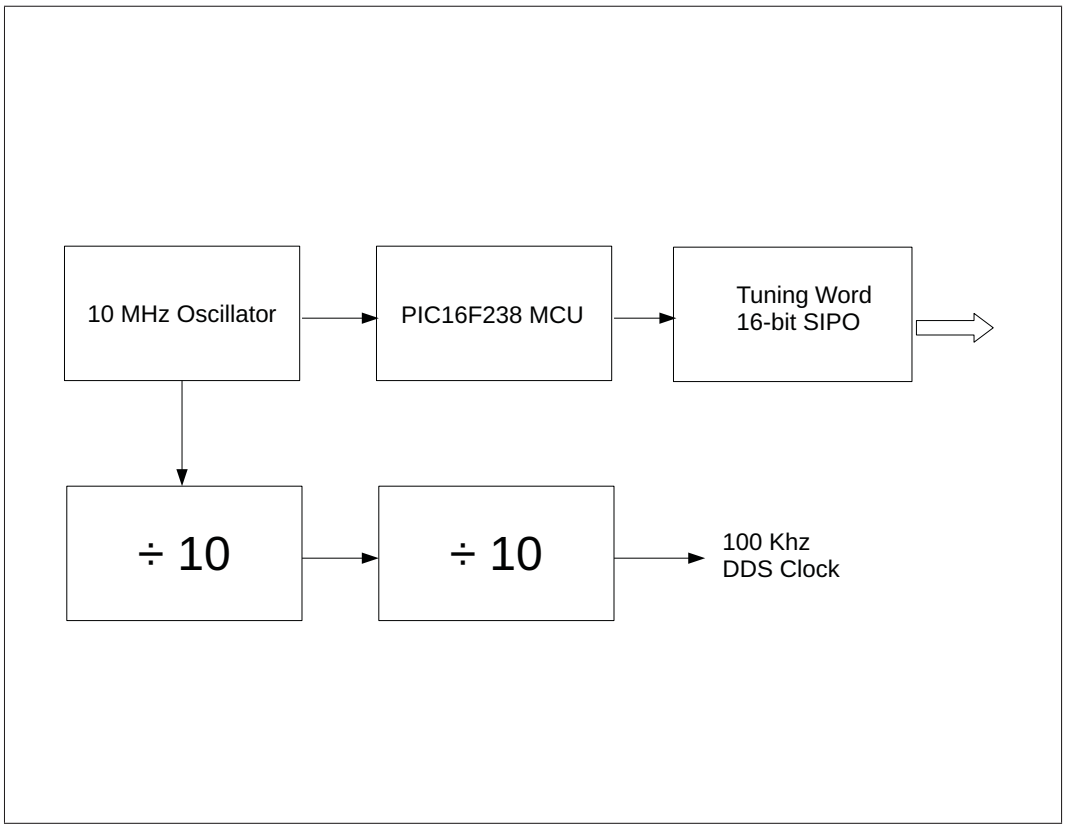
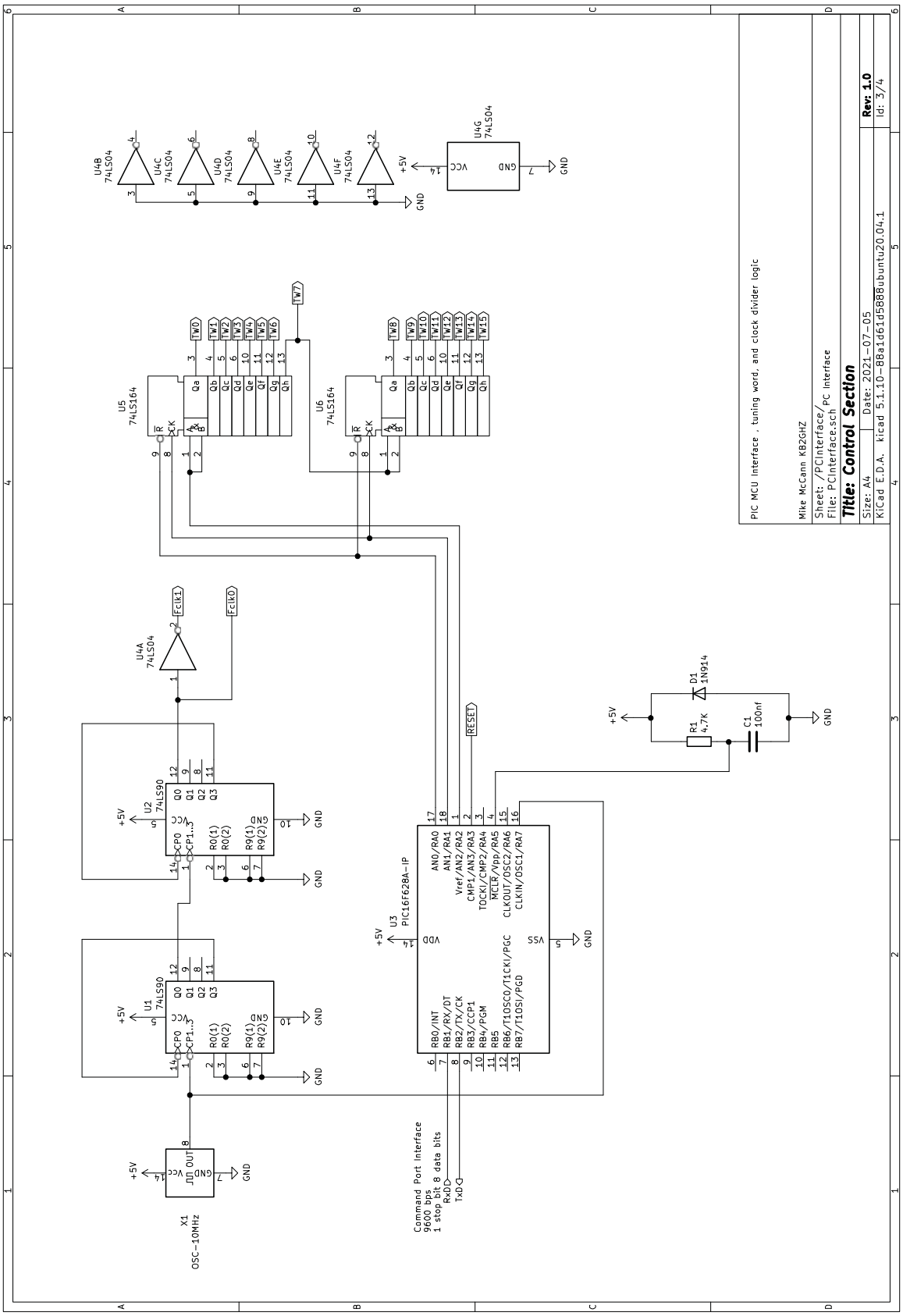


Figure 4: Control Section Block Diagram

Figure 5: Control Section Schematic



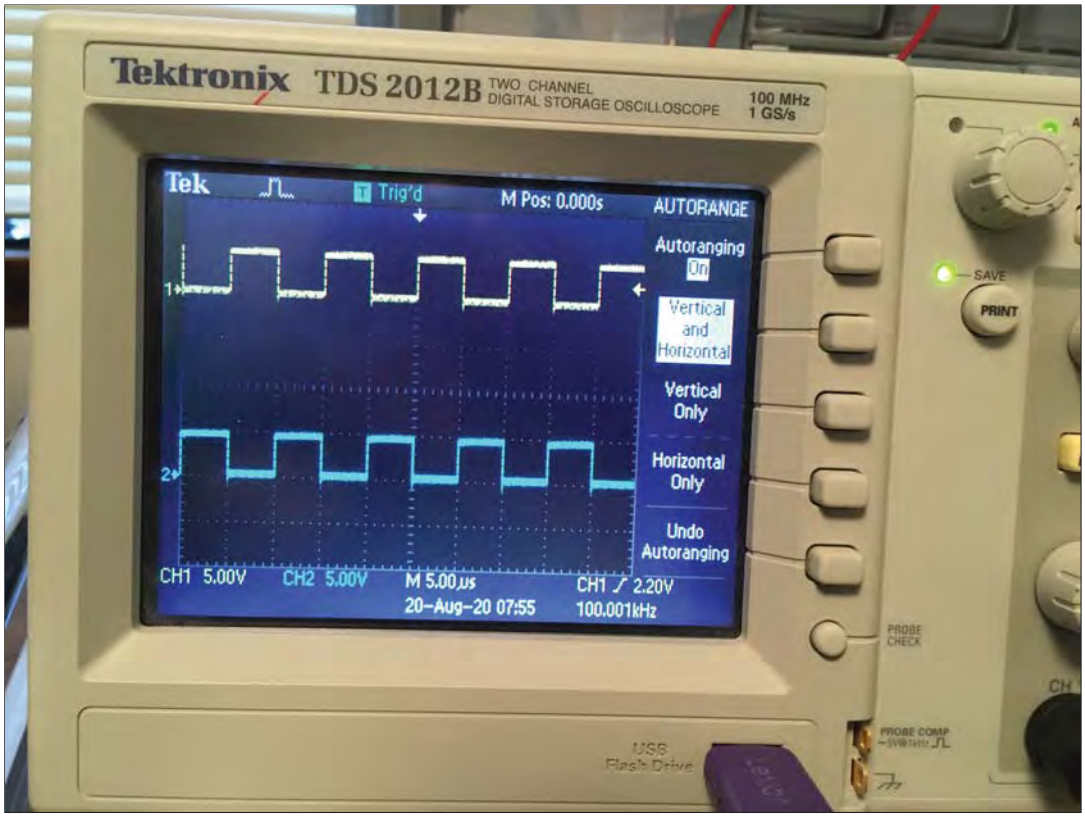


Figure 6: 100 kHz DDS Clock

2.2 Phase Accumulator

Figure 7 illustrates the organization of the phase accumulator circuit. The 16-bit adder is implemented using four 74LS283 4-bit adder ICs. Ripple carry is accomplished by connecting the C4 output to the C0 between adder stages. For each 74LS283 IC, port A is connected to the tuning word register, and port B is connected to 16-bit accumulator's output. The 16-bit accumulator is implemented using four 74LS273 8-bit Octal D flip-flop ICs. The four ICs are arranged as two 16-bit registers in a master-slave arrangement. Data is latched in to the master and slave sections using the two-phase 100 kHz clock signal generated by the control section. This arrangement is necessary to avoid a race condition where the output from the 16-bit adder conflicts with the current phase accumulator value.

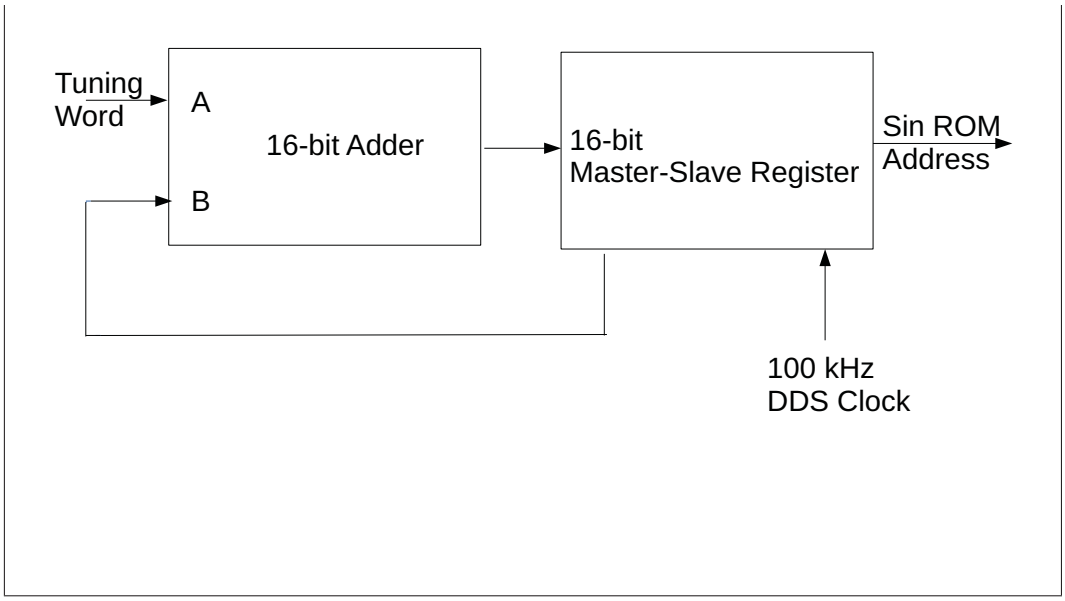
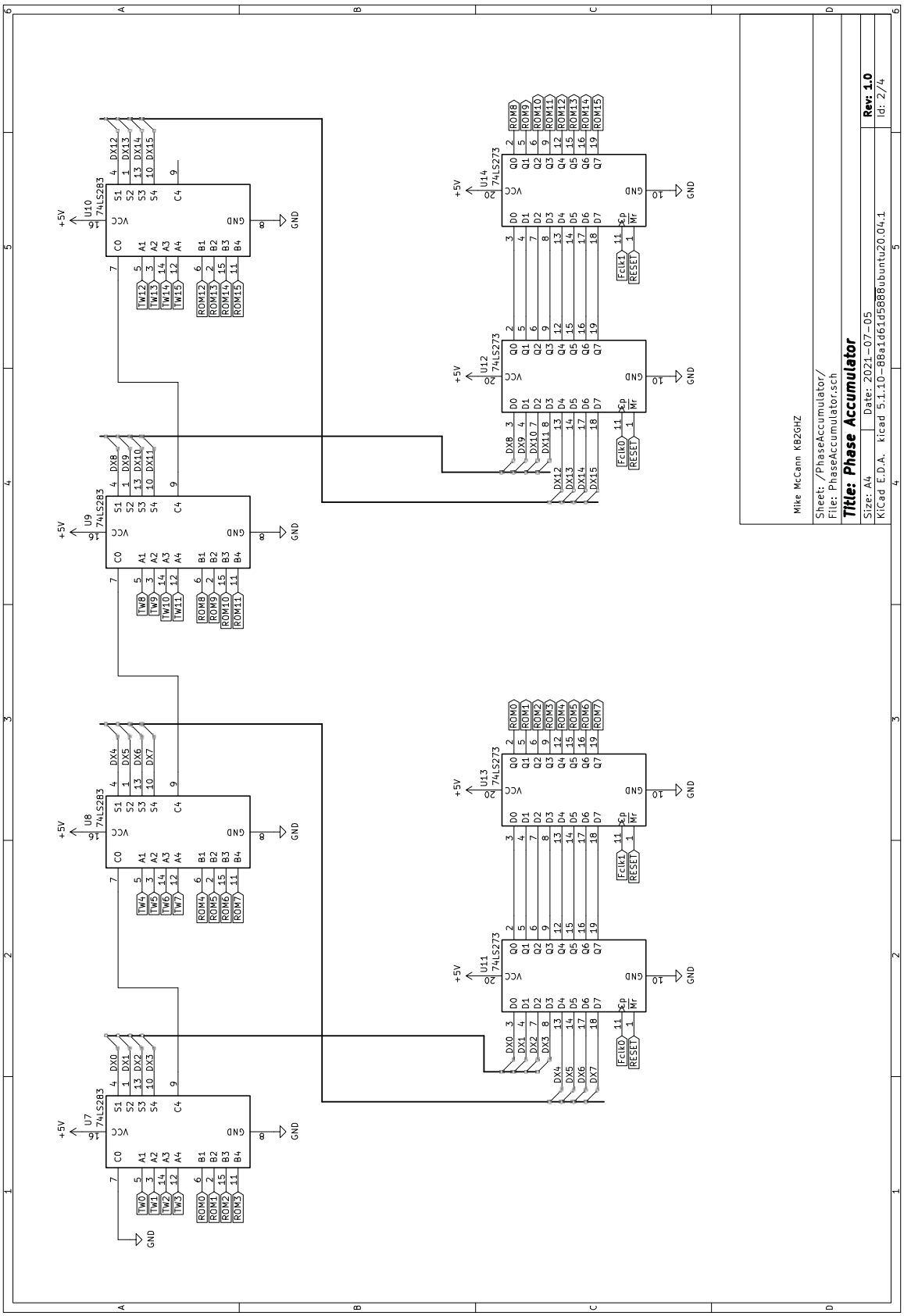


Figure 7: Phase Accumulator Block Diagram

Figure 8: Phase Accumulator Schematic



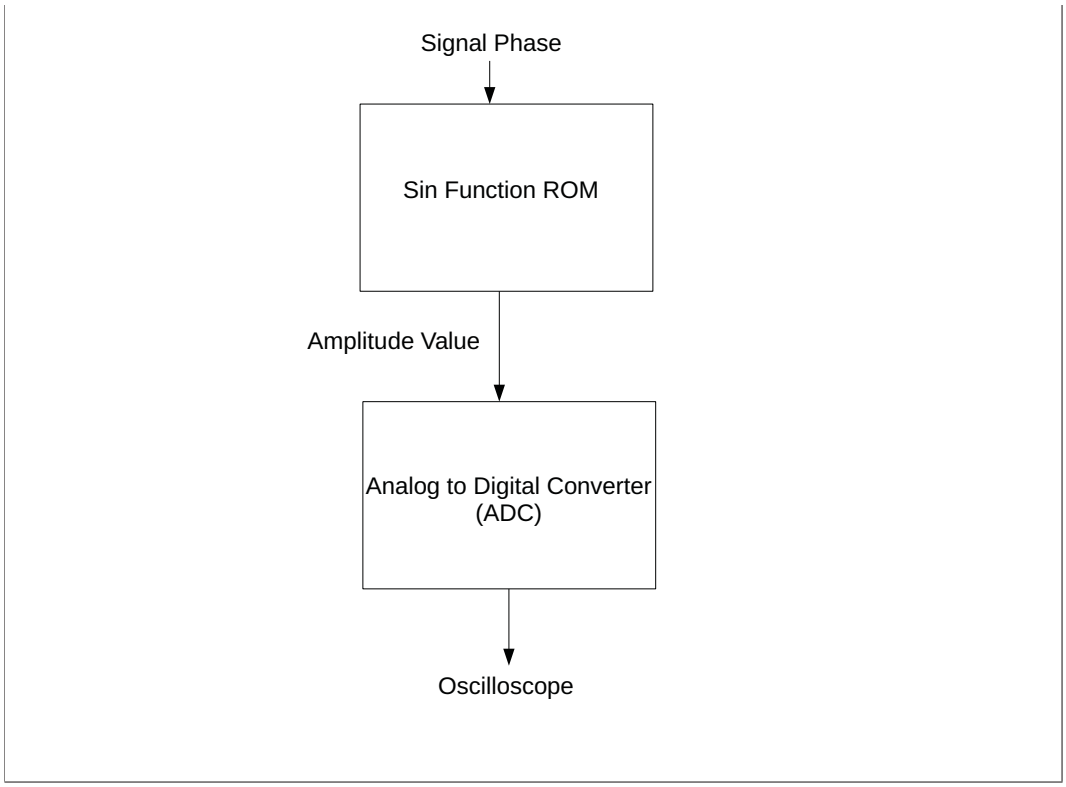
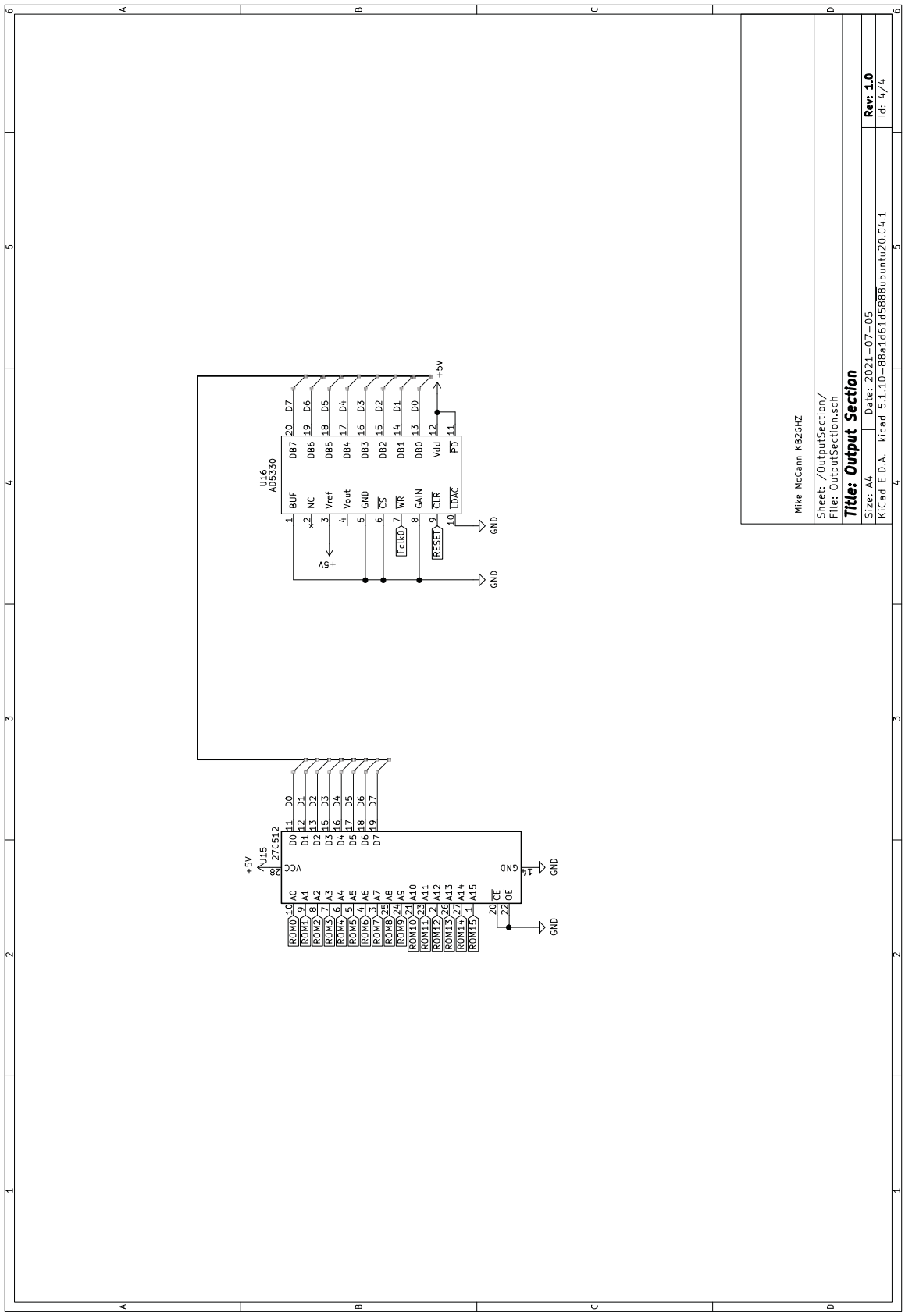


Figure 9: Output Section Block Diagram

2.3 Output Section

Figure 9 depicts the DDS output section. The signal phase output from the phase-accumulator is applied to the address bus of the Sine function ROM. The data bus outputs of the 27C512 ROM are then routed to the Analog Devices AD5330 Digital to Analog Converter Module (DAC). The DAC module executes an digital to analog conversion each time the $F_{clk}0$ signal makes a high to low transition.

Figure 10: Output Section Schematic



3 Construction and Operation

Figure 11 below is a photograph of the completed DDS project assembled on a solder-less breadboard. The IC in the upper right corner is the PIC16F628A-IP micro-controller, the silver package below the PIC micro-controller is the 10 MHz clock oscillator. The two ICs below the oscillator are 74LS90 dividers configured for divide by 10 operation. These ICs provide the 100 kHz DDS clock signals (F_{clk0} and F_{clk1}). The two ICs at the top of the 2nd column from the left are 74LS164 SIPO devices that comprise the 16-bit tuning word register. The four ICs below the tuning word register (74LS283 4-bit adders) are the phase accumulator's 16-bit adder. The four ICs in the 3rd column from the left (74LS273) are the phase accumulator's 16-bit accumulator. The IC located in the upper right hand corner is the Sine function ROM (27C512). The red circuit board below the ROM is an Analog Devices AD5330 DAC IC evaluation board. A complete set of KiCad files and schematics are available on github at `https://github.com/kb2ghz/DDS`.

Setting the DDS output frequency is a two step process. First, the tuning word value needs to be calculated. I coded a simple Python program (freqcalc.py) to calculate the hexadecimal value needed to set the frequency. The the desired frequency is set by using sending "FXXXX", where XXXX is the tuning word value in hex, to the DDS at 9600 baud. Figure 12 below shows the output frequency being set to 100 Hz. Figure 13 shows the 100 Hz output signal on an oscilloscope.

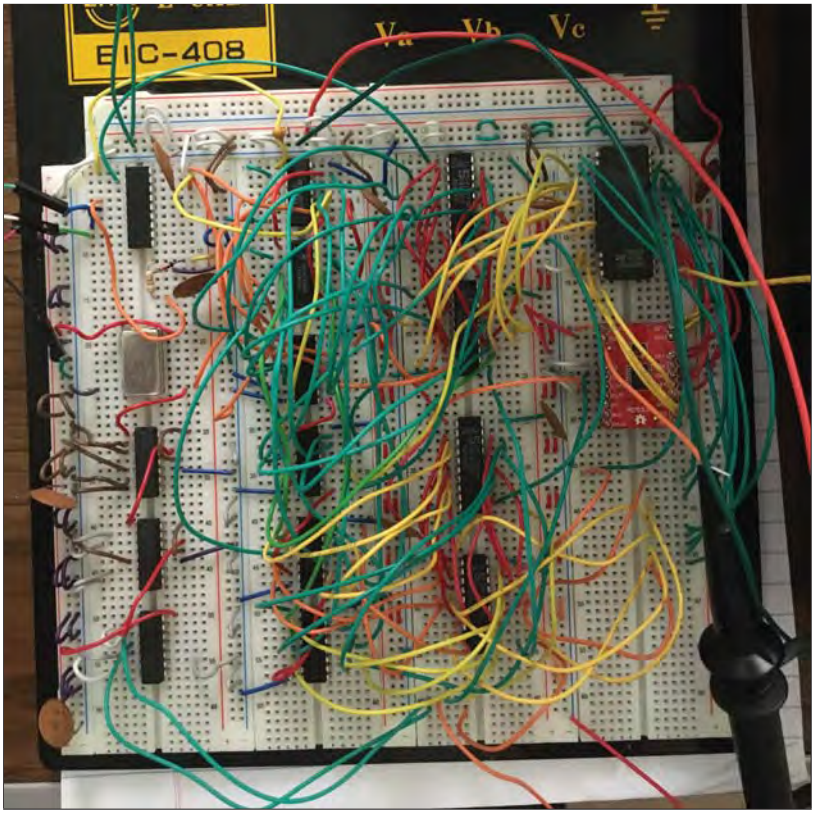


Figure 11: Breadboard DDS Circuit

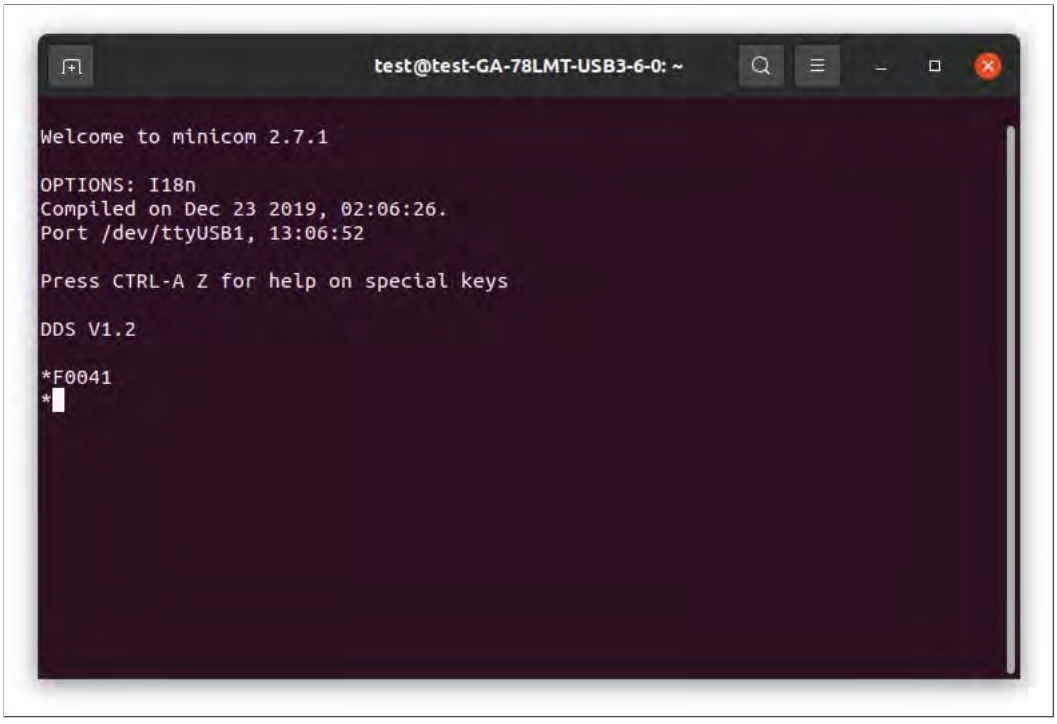


Figure 12: Setting the DDS Frequency

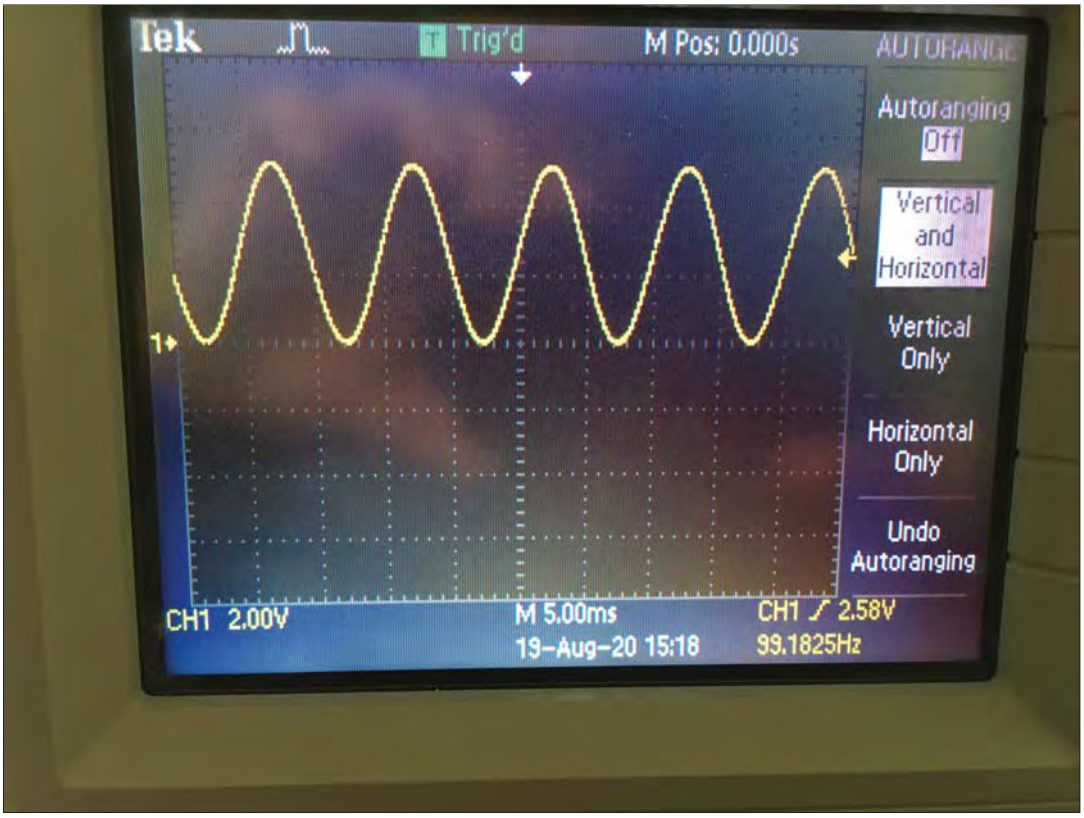


Figure 13: DDS Output Signal