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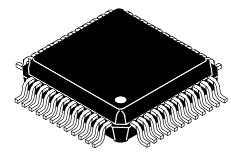
MC145750

Product Preview

QPSK Encoder

The MC145750 is a silicon gate HCMOS device designed to encode π/4–shift QPSK baseband signals. The device contains two 10–bit DACs for the I/Q signal, Root–Nyquist digital filtering, and burst rising and falling edge processing for digital RF communication equipment. Primary applications for this device are in products that will be used in PHS (384 kbps) and PDC (42 kbps). It will perform up to 800 kbps data rate. It also contains PN511 random pattern generator and timing generator with PLL.

- Root–Nyquist Digital Filtering (Coefficient = 0.5)
- Burst Edge Processing Circuitry (Ramp–Up and –Down)
- Two 10–Bit DACs for I/Q Output
- Operating Voltage Range: 2.7 to 5.5 V
- PN511 Random Pattern Generator
- Conformance to RCR Standard for PHS, PDC
- Variable Data Transmission Rate up to 800 kbps (V_{DD} = 5 V)
- Timing Generator with PLL
- QPSK Mode, Burst, and Continuous I/Q Signal Output is Performed
- Companion Device is MRFIC0001

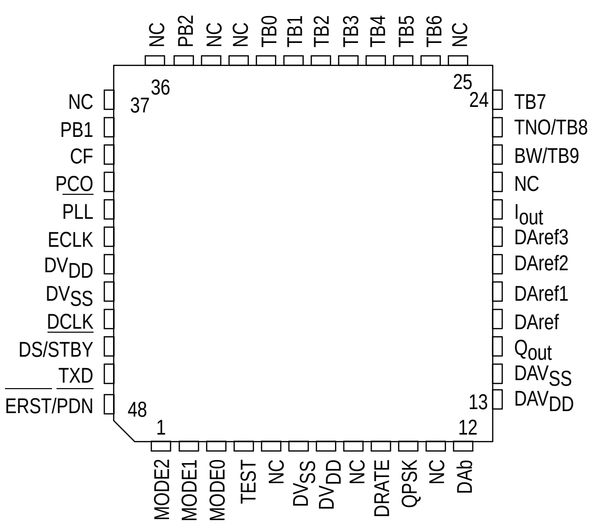


VFU SUFFIX
PLASTIC VQFP
CASE 932

ORDERING INFORMATION

MC145750VFU VQFP

PIN ASSIGNMENT

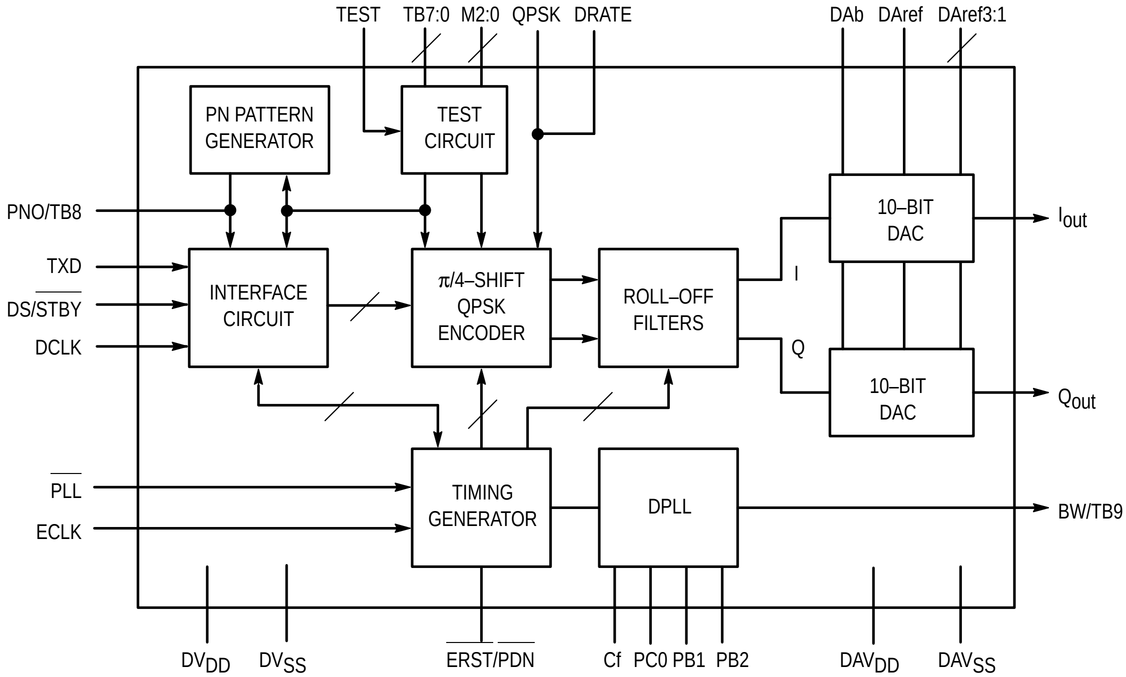


NC = NO CONNECTION

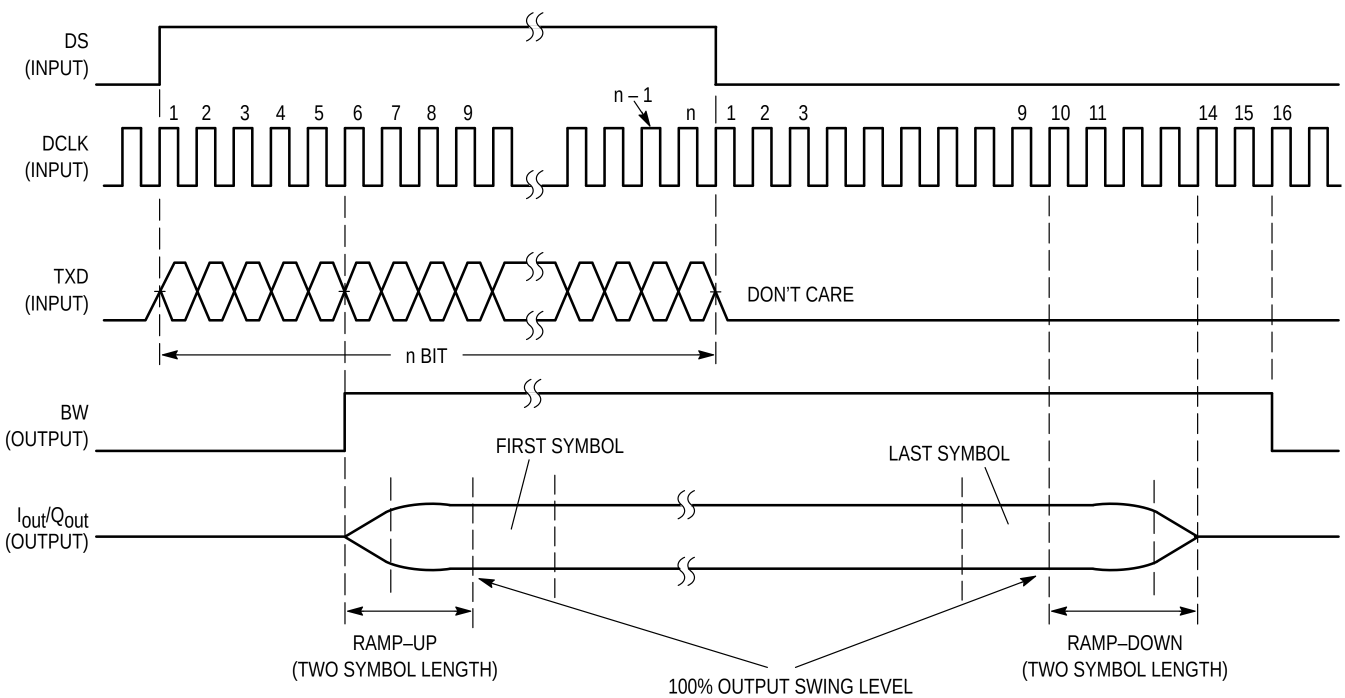
This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

REV 2
10/95

BLOCK DIAGRAM



INPUT/OUTPUT TIMING RELATIONS



MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	– 0.5 to + 7	V
DC Input Voltage	V_{in}	– 0.5 to V_{DD} + 0.5	V
Power Dissipation	P_D	500	mW
Storage Temperature	T_{stg}	– 65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
DC Supply Voltage	V_{DD}	2.7	3.3	5.5	V
DC Input Voltage	V_{in}	0	—	V_{DD}	V
Operating Temperature Range	T_A	– 20	25	85	°C

ELECTRICAL CHARACTERISTICS (T_A = 25°C, TXD = L, Normal Mode)

Parameters		Symbol	Condition	Min	Typ**	Max	Unit
DC Supply Current V_{DD} = 3 V		I_{dd1}	$\overline{ERST}$ = L	—	0.25	0.5	mA
	DRATE = L	I_{dd2}	DS = L	—	5.0	6.0	
	DRATE = H	I_{dd3}		—	1.5	1.8	
	DRATE = L	I_{dd4}	DS = Burst Input*	—	5.0	6.0	
	DRATE = H	I_{dd5}		—	1.5	1.8	
	DRATE = L	I_{dd6}	DS = Continual Input	—	8.0	10.0	
	DRATE = H	I_{dd7}		—	2.0	2.6	
DC Supply Current V_{DD} = 5 V		I_{dd1}	$\overline{ERST}$ = L	—	0.5	3.0	mA
	DRATE = L	I_{dd2}	DS = L	—	27.0	33.0	
	DRATE = H	I_{dd3}		—	17.0	19.0	
	DRATE = L	I_{dd4}	DS = Burst Input*	—	30.0	33.0	
	DRATE = H	I_{dd5}		—	18.0	20.0	
	DRATE = L	I_{dd6}	DS = Continual Input	—	33.0	37.0	
	DRATE = H	I_{dd7}		—	18.0	20.0	

* 625 µs burst/5 ms period (DRATE = L) at DCLK = 384 kHz.
6.6 ms burst/20 ms period (DRATE = H) at DCLK = 42 kHz.
** Typical numbers are not guaranteed.

ANALOG CHARACTERISTICS (T_A = 25°C)

Parameters		Symbol	Condition	Min	Typ**	Max	Unit
Output Swing Level I/Q Out	V_{DD} = 3 V	V_{out}	RL = kΩ, TXD = L Normal Mode	500	550	600	mV p–p
	V_{DD} = 5 V			520	570	620	
Output Swing Imbalance		ΔV_{out}		– 0.5	0	0.5	dB
Output DC Level I/Q Out	V_{DD} = 3 V	V_{out}	DS = L	800	820	840	mV
	V_{DD} = 5 V			780	800	820	
Output Swing Imbalance		ΔV_{DD}		—	—	20	
Out–of–Band Noise Level	V_{DD} = 5 V	V_{in}	600 kHz	—	– 50	—	dB
			900 kHz	—	– 55	—	
DC Output Resistance		R_{out}	I_{out}/Q_{out}	—	50	100	Ω

* DAref1 = H at V_{DD} = 3 V, DAref3 = H at V_{DD} = 5 V
** Typical numbers are not guaranteed.

SWITCHING CHARACTERISTICS (T_A = 25°C)

Parameters		Symbol	Condition	Min	Typ*	Max	Unit
Input Voltage	High–Level	V_{IH}		V_{DD} x 0.7	—	—	V
	Low–Level	V_{IL}		—	—	V_{DD} x 0.3	
Output Voltage	High–Level	V_{OH}	BW, PNO	V_{DD} x 0.9	—	—	
	Low–Level	V_{OL}		—	—	V_{DD} x 0.1	
Data Set–Up Time		t_{su}	TXD, DS, STBY	10	—	—	ns
Data Hold Time		t_h	TXD, DS, STBY	10	—	—	
Data Output Propagation Delay		t_{pd}	BW, PNO	—	1.5	3	µs
I/Q Output Propagation Delay		T_D	I_{out}, Q_{out}	—	4	6	
Data Rate	V_{DD} = 3 V		DRATE = L	—	—	450	kbps
			DRATE = H	—	—	55	
	V_{DD} = 5 V		DRATE = L	—	—	800	
			DRATE = H	—	—	100	
Clock Input Duty Cycle		DCLK		45	50	55	%
VCO Oscillation Frequency	V_{DD} = 3 V	f_{VCO1}		—	—	20	MHz
	V_{DD} = 5 V	f_{VCO2}		—	—	32	

* Typical numbers are not guaranteed.

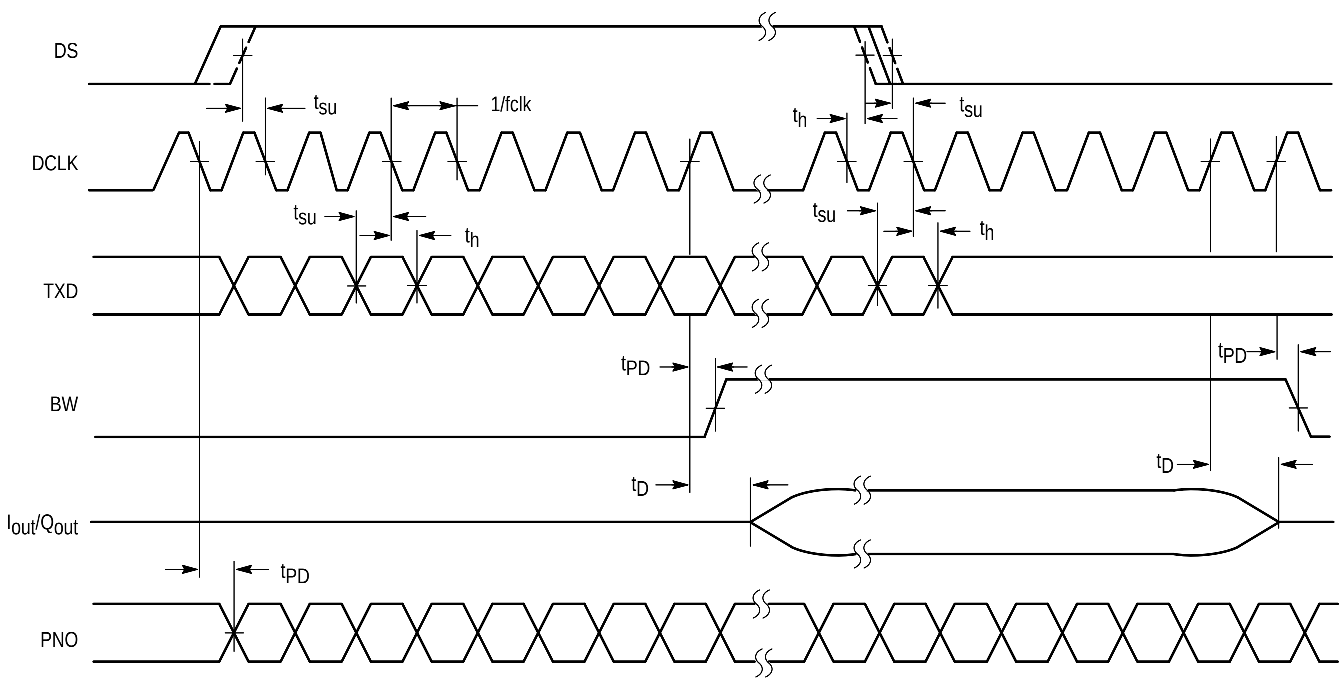


Figure 1. Timing Diagram

PIN DESCRIPTIONS

POWER SUPPLY

V_{SS}
Digital Ground (Pins 6, 44)

These are the negative power supply input pins to the digital portion of the device and are connected to ground (0 V).

V_{DD}
Positive Power Supply Input (Pins 7, 43)

These are the positive power supply input pins to the digital portion of the device. Typical operating voltage range is 3.3 V at DAref3 = H, 5.0 V at DAref1 = H. Power should be fed simultaneously with DAV_{DD} pin in order to avoid any possible damage to the device.

DAV_{DD}
Positive Power Supply Input for DACs (Pin 13)

This is the positive power supply input pin to the analog portion of the device. Typical operating voltage range is 2.7 V to 5.5 V.

DAV_{SS}
Analog Ground for DACs (Pin 14)

This is the negative power supply pin to the analog portion of the device and is connected to ground.

MODE CONTROL AND TEST

MODE0 – MODE2
Normal/Test Mode Select (Pins 1, 2, 3)

These pins must be connected to ground for normal operation. For system test, PN pattern generation mode will be performed when MODE0 = H and MODE1, MODE2 = L. PN511 signal is fed to the encoder instead of input data from TXD pin. Data shift timing is the same as the normal operation mode and burst timing indicated by DS pin is still valid for the device. The PN511 signal is monitored at the PNO pin.

TEST
Test Mode (Pin 4)

The device operates normally while this pin is held low. When this signal is high, the device enters into factory test mode. Only one mode is allowed to be enacted by user for PN Mode.

DRATE
Data–Rate Select (Pin 9)

This pin can select high data rate when it is low, such as in PHS applications.

QPSK
(D)QPSK/π/4–Shift QPSK Mode Select (Pin 10)

The device operates as a π/4–QPSK Encoder when this pin is held high. By making this pin low, it functions as non–shift differential QPSK Encoder. All of the functions are the same in both modes.

PN0/TB8
PN511 Test Pattern Output/Test Bus 8 (Pin 23)

This is the output data of PN511 test–pattern in normal mode. When the PN pattern generator outputs to this pin, it can be output I/Q pins and data from TXD pin may be ignored. If the DS signal is L, I/Q pins stop but PN data stream may be output.

TB0 – TB7
Test Bus (Pins 24, 26 – 32)

These pins are used in factory test and should be connected to ground for normal operation.

PLL
Int/Ext PLL Clock Select (Pin 41)

When this pin is connected to ground, the PLL is active and timing will be generated internally. When this pin is connected to V_{DD}, timing should be applied to the ECLK pin.

DIGITAL INTERFACE PINS

BW/TB9
Burst Window Output/Test Bus 9 (Pin 22)

This output indicates when modulated baseband I/Q signals are output from this device. This pin is used as the transmission control signal for saving power for RF.

ECLK
External Clock Input (Pin 42)

When the internal timing generator with PLL is not used in the system, this pin must have 15.36 MHz applied as a system clock for this device. This pin is connected to ground for normal operation.

DCLK
Data Shift Clock Input (Pin 45)

This is the shift clock input for the transmit data input and is typically 384 kHz for the PHS (DRATE Pin = L) and 42 kHz for the PDC (DRATE Pin = H) application. The data input occurs at the rising edge of the DCLK. For burst–type systems such as the TDMA data transmission applications, this signal must be synchronized with the rising/falling edge of the DS pin (Data Slot Timing Input).

DS/$\overline{\text{STBY}}$
Data Slot Timing/Standby Input (Pin 46)

For burst–type, this input signal indicates when transmit data are valid for the device. Its duration must be equal with the number of input data to the device, and its transition must be aligned with the rising edge of the DCLK signal.

When a logic L is applied to this pin, all digital portions except the timing generator are not clocked and the device is in a low power dissipation mode. When a logic H is applied continuously, all input data are encoded as valid data.

TXD
Transmit Data Input (Pin 47)

Data bit streams to be transmitted are input to this pin. The data is valid only when the DS (Pin 46) is asserted (high). Its transition should be synchronized with rising edge of the DCLK (Pin 45).

$\overline{\text{ERST}}/\overline{\text{PDN}}$
External Reset/Power Down Input (Pin 48)

When a logic L is applied to this pin, it forces a complete power down. When at start up, V_{DD} goes high, it is recommended that a logic L, then a logic H be applied to this pin to start up and reset all digital portions.

ANALOG INTERFACE PINS

Q_{out}
Filtered Quadrature–Phase Output (Pin 15)

This is the modulated quadrature–phase signal output and the amplitude is typically 550 mV p–p at V_{DD} = 3 V in PN test mode. The output dc resistance is approximately 50 Ω.

I_{out}
Filtered In–Phase Output (Pin 20)

This is the modulated in–phase signal output and amplitude is typically 500 mV p–p at V_{DD} = 3 V in PN test mode. The output dc resistance is approximately 50 Ω.

DAC AND PLL SETTING

DAb
Reference Bias Setting Pin to DACs (Pin 12)

A resistor connected to ground from this pin determines the reference current value for internal DACs. This resistor's value is 200 kΩ typically.

DAref
Ripple Filter Capacitor (Pin 16)

A capacitor connected to ground from this pin acts as a ripple filter for the internal DACs' reference voltage. This capacitor's value is 0.1μF, typically.

DAref1 – DAref3
Reference Bias Setting to DACs (Pin 17 – 19)

These pins determine the reference voltage for internal DACs in conjunction with DAb pin. At 3 V operation, DAref1 pin should be connected to V_{DD}. DAref2 pin should be connected to V_{DD} at 3.3 V. DAref3 pin should be connected to V_{DD} at 5 V. The two other pins for the respective cases must be left open.

PB1, PB2
PLL Bias (Pins 35, 38)

This pin determines the bias of the PLL. Its recommended values are shown in Table 1 and it depends on operating voltage.

Cf
Loop Filter Capacitor (Pin 39)

Input from Cf pin is fed directly as the internal VCO control signal.

PCO
Phase Comparator Output (Pin 40)

Connect an LPF as loop filter for the PLL. Refer to the application figure for recommended values.

Table 1. Function Table

Pin		L	H	Remarks
3	MODE0	Normal Mode	PN Pattern	These settings are independent of power supply.
10	QPSK	Non–Shift	/4–Shift	
9	DRATE	High Speed	Low Speed	To be determined setting high or low speed data rate.
17	DAref1	—	V_{DD} = 5 V	These pins should be held high depending on power supply voltage and others should be left open.
18	DAref2	—	V_{DD} 3.3 V	
19	DAref3	—	V_{DD} 3.0 V	
41	$\overline{\text{PLL}}$	PLL Operation Mode	Ext Clock Mode	In case of external clock mode, TX data rate must be set to a frequency of 1/40 when DRATE = L, and must be set to a frequency of 1/320 when DRATE = H. Max data rate is limited by power supply.
48	$\overline{\text{ERST}}/\overline{\text{PDN}}$	Power Down	Normal Operation	Digital circuits reset condition will be released by rising edge of this input.

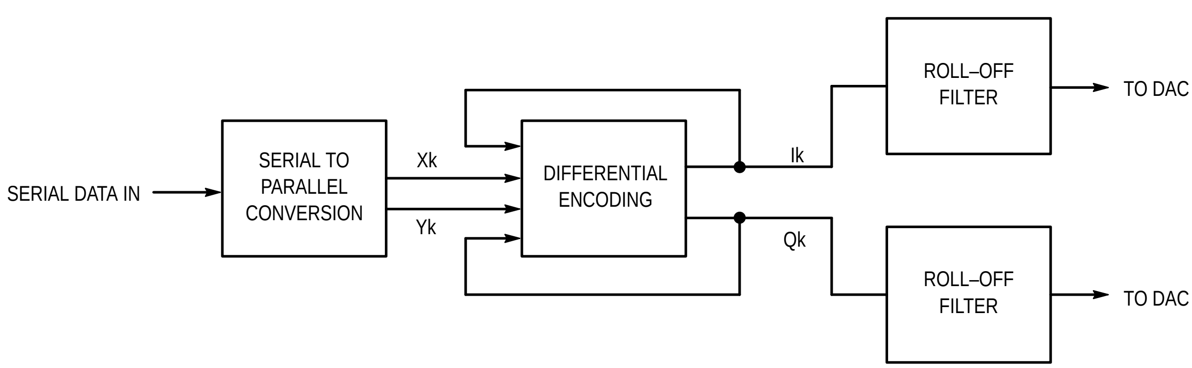


Figure 2. DQPSK Baseband Signal Generation

DEVICE DESCRIPTION

π/4–Shift QPSK Encoding

RCR standard (STD–28) specifies the basic configuration of this modulation scheme as shown in Figure 2. First, serial data input is converted to Xk/Yk parallel streams. Then its value is compared with one previous symbol Ik/Qk, respectively, whether or not there is a change of polarity. If there is a change, result is coded as 1. This two–bit πr (di–bit) is called symbol, hence symbol rate is just half of the data input rate to be modulated.

Phase transitions are determined as shown in Figure 3, with respect to four di–bit values of Xk, Yk. (As is shown, there should be at least π/4 of phase shift in each symbol timing unlike plain QPSK.) Actual in–phase outputs are fed to a quadrature modulator circuit, and it is recommended that a 2– to 3–order LPF be used, which may be used as a level shifter and dc offset compensation circuitry at the same time.

The reference voltage for the DACs is given by connecting either of DAref1:3 to V_{DD} according to the operating voltage used. It is preferable not to have this voltage vary, since I/Q output levels are affected.

Timing Generator

The PLL is intended in order to generate all required timing signals for the devices. The VCO oscillating at the PN511 pattern rate is utilized when some characteristics are measured. By pulling MODE0 pin high, the device generates this sequence. It is a useful simple measurement for the occupied power bandwidth and the out–of–band power level. The sequence itself can also be monitored at the PNO pin.

This circuit is reset by an external reset signal while the low–state of DS is not valid for initializing the generator.

START–UP SEQUENCE

To ensure stability and to initialize the internal ROM and encoder, the start–up sequence should be done at power–up. Refer to Figure 4.

Di–Bit Input

Xk	Yk	Phase Shift
0	0	π/4
0	1	3π/4
1	0	– π/4
1	1	– 3π/4

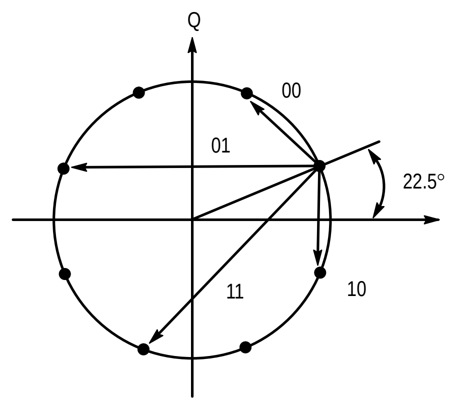


Figure 3. Phase Diagram

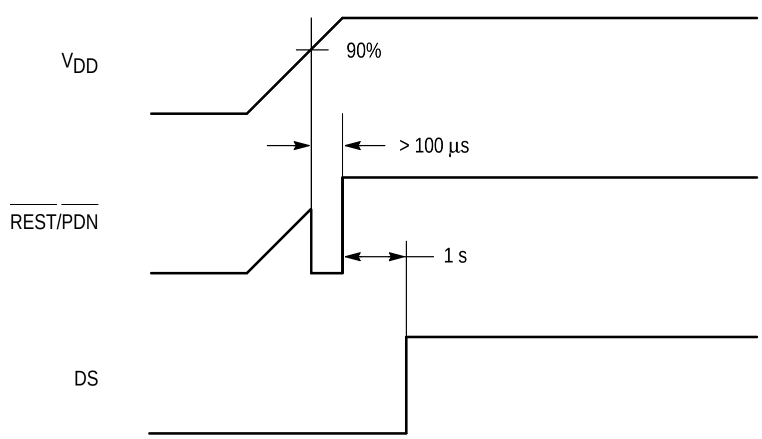


Figure 4. Start–Up Sequence

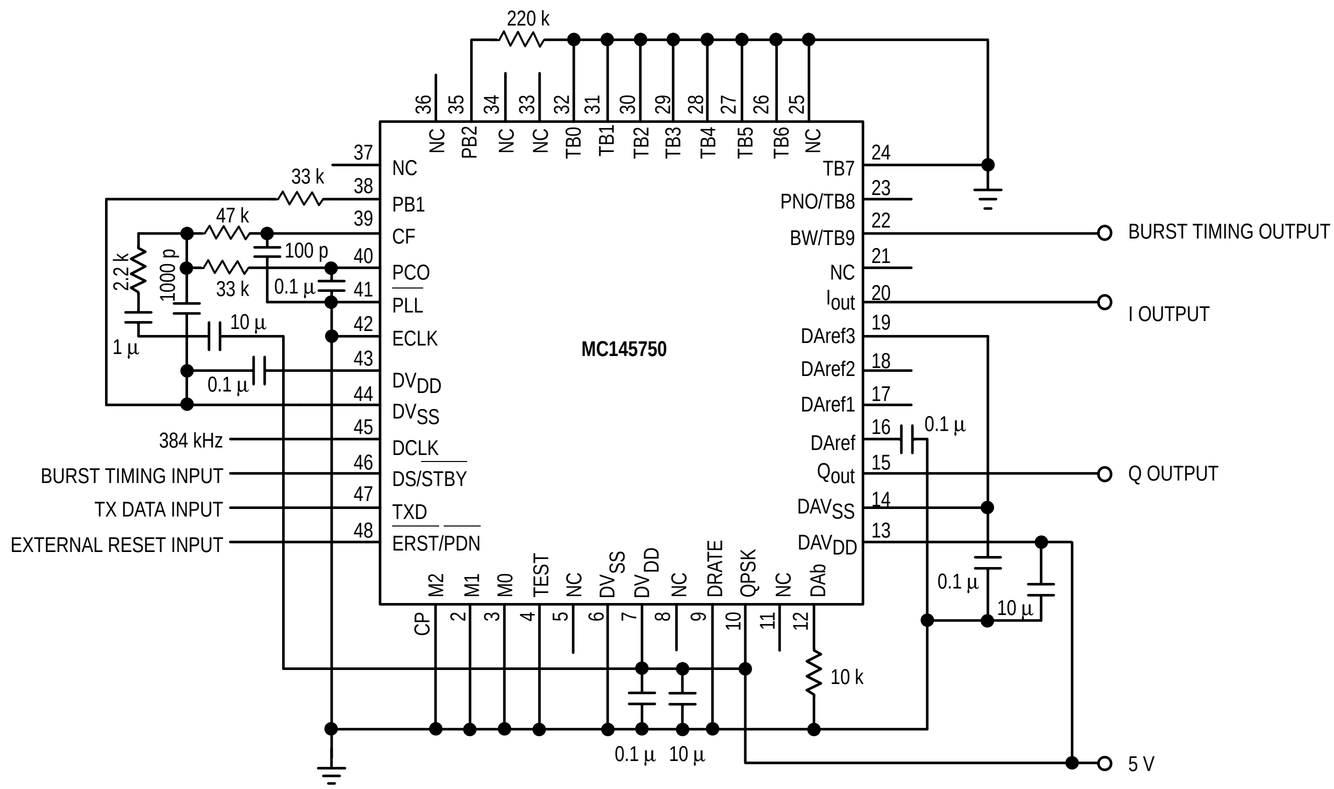


Figure 5. DRATE Equals L: 5 V Operation

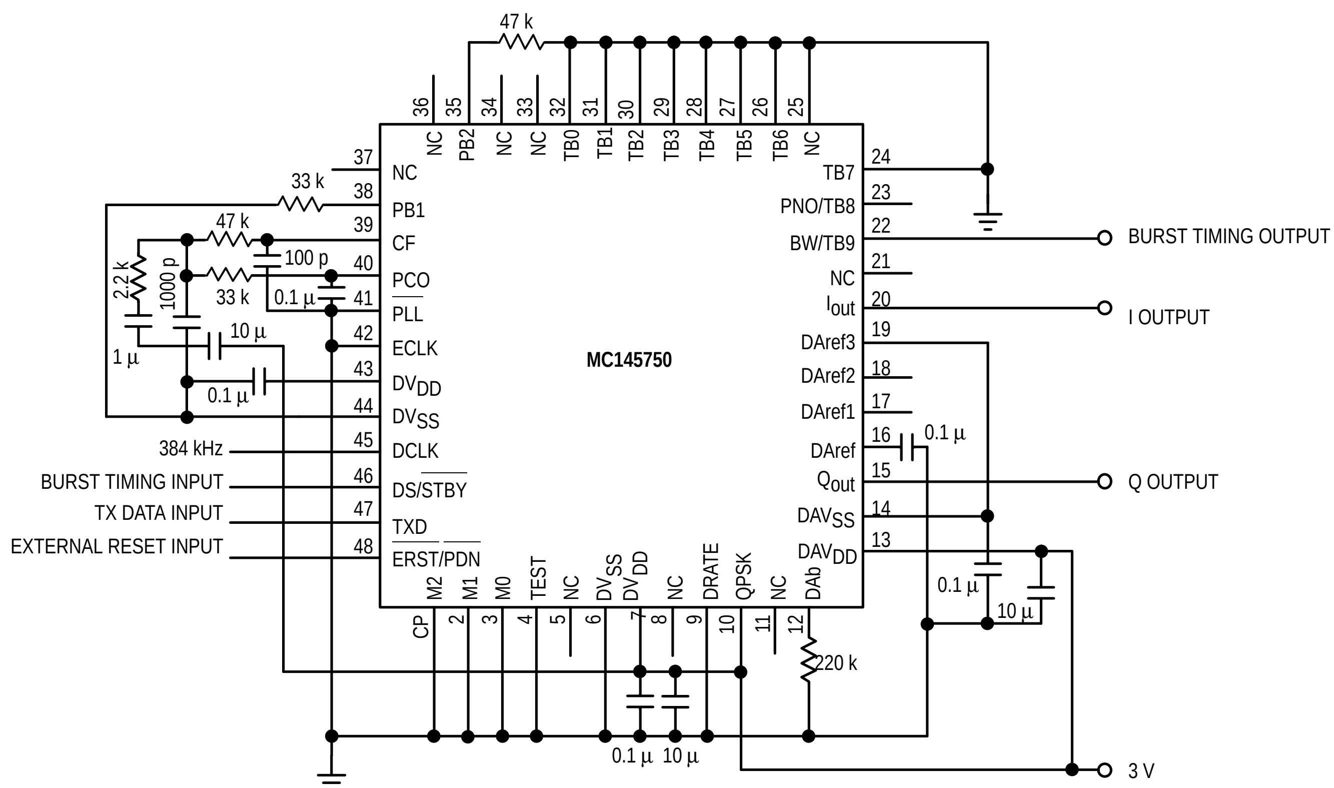


Figure 6. DRATE Equals H: 3 V Operation

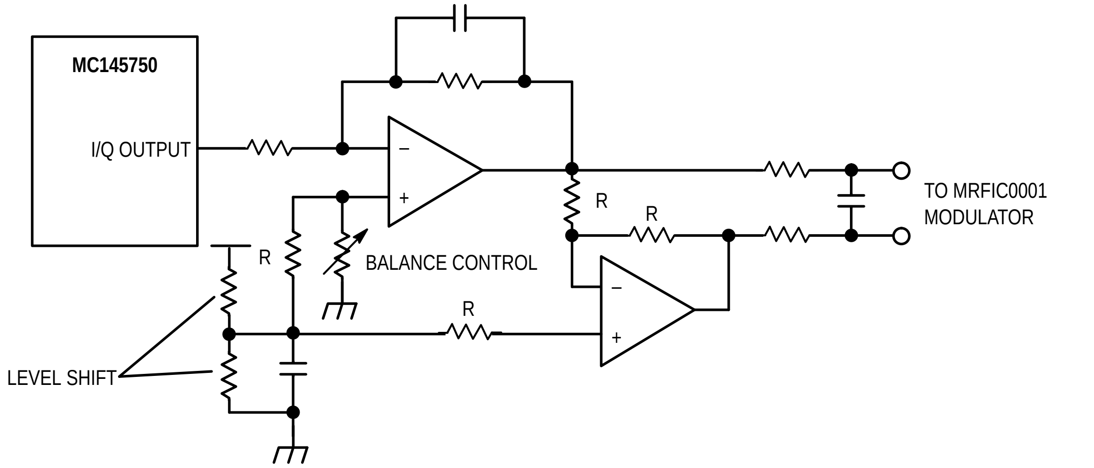


Figure 7. I/Q Output Interface Circuit 1

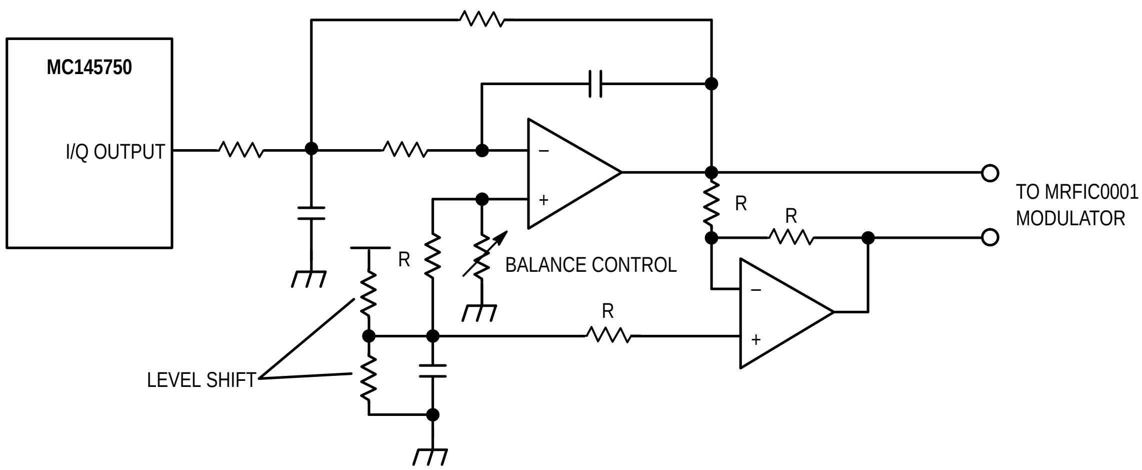
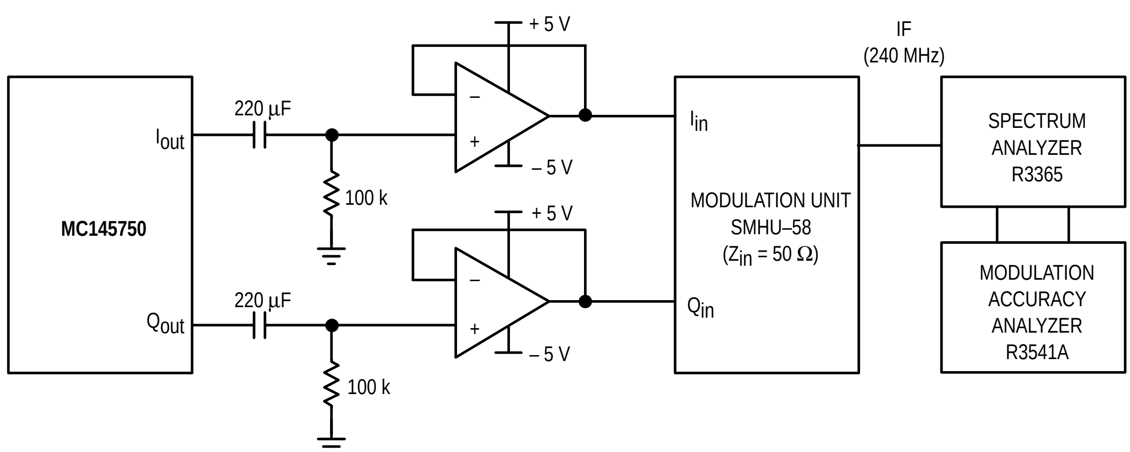


Figure 8. I/Q Output Interface Circuit 2



Measurement Equipment:	Advantest Spectrum Analyzer R3365 Advantest Modulation Accuracy Analyzer R3541A Rohde & Schwarz Modulation Unit SMHU–58
Conditions:	Internal PLL mode, 384 kbps (PHS), T_A = 25°C

Motorola cannot recommend one supplier over another and in no way suggests that this is a complete listing of measurement equipment suppliers.

Figure 9. Modulation Accuracy Measurement Schematic

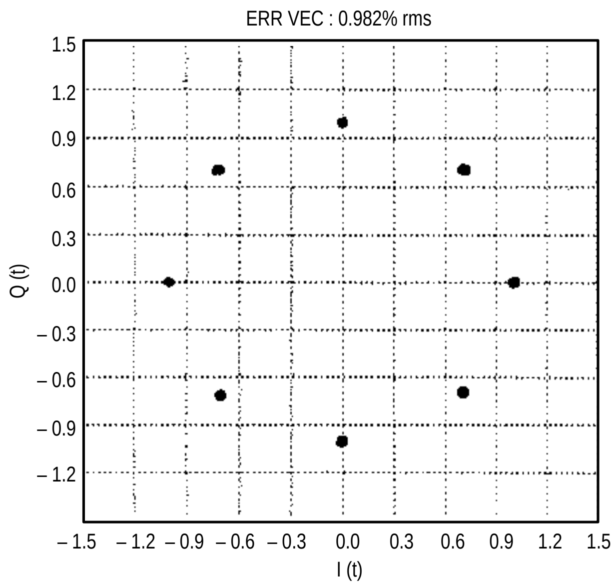


Figure 10. I–Q Pattern

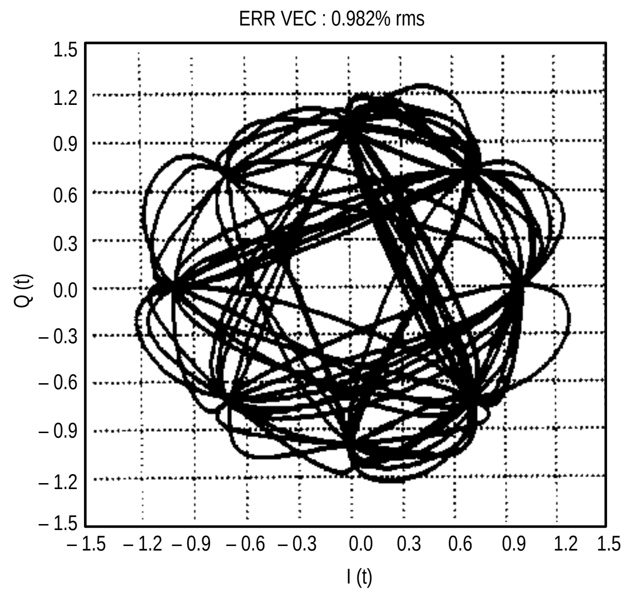


Figure 11. I–Q Pattern

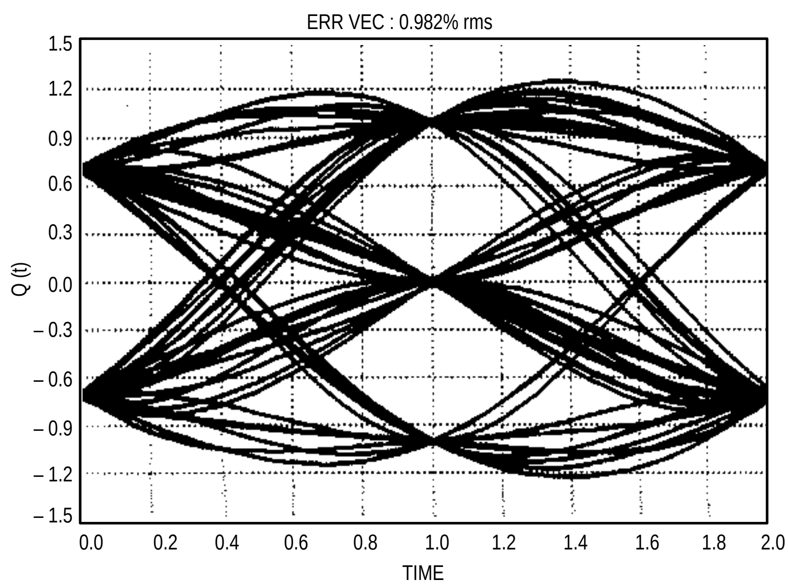
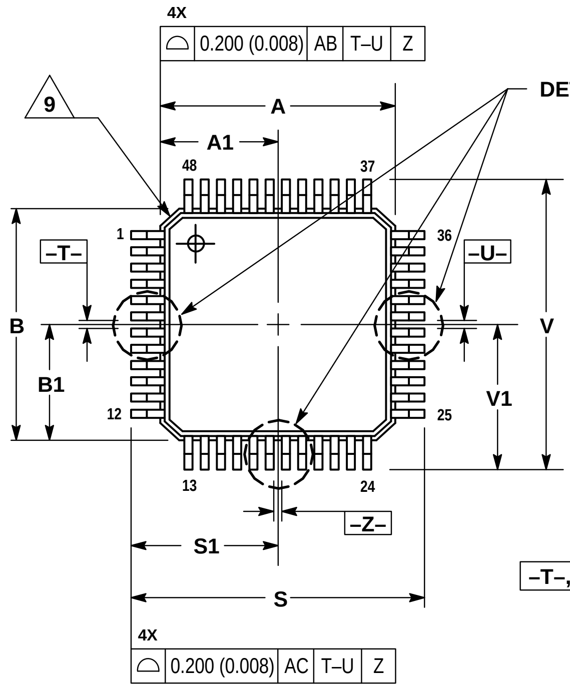
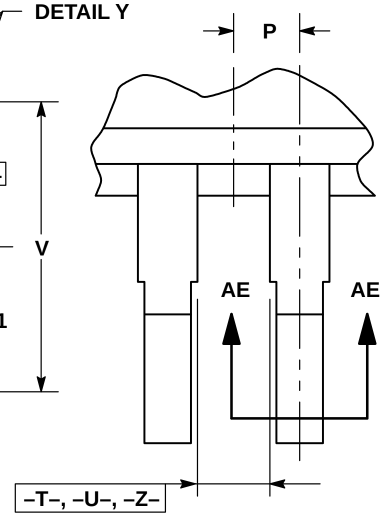


Figure 12. Q–Eye Pattern

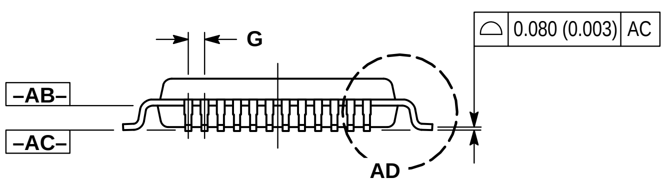
PACKAGE DIMENSIONS

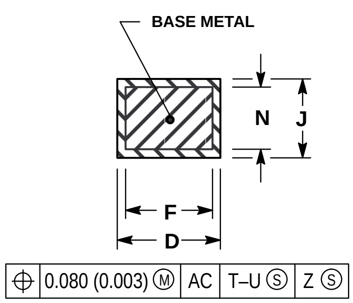
VFU SUFFIX
PLASTIC VQFP
CASE 932–02



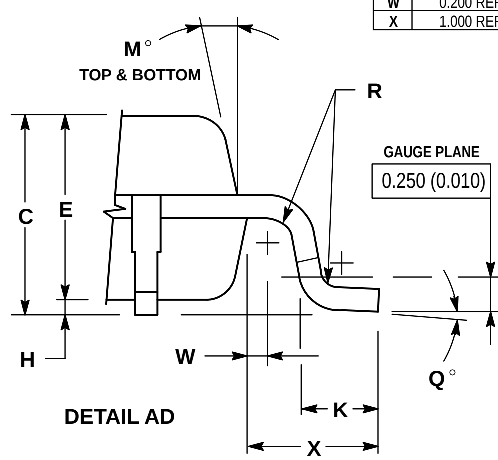


DETAIL Y





SECTION AE–AE



DETAIL AD

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE –AB– IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS –T–, –U–, AND –Z– TO BE DETERMINED AT DATUM PLANE –AB–.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE –AC–.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.250 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE –AB–.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE D DIMENSION TO EXCEED 0.350 (0.014).
8. MINIMUM SOLDER PLATE THICKNESS SHALL BE 0.0076 (0.0003).
9. EXACT SHAPE OF EACH CORNER IS OPTIONAL.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	7.000 BSC		0.276 BSC	
A1	3.500 BSC		0.138 BSC	
B	7.000 BSC		0.276 BSC	
B1	3.500 BSC		0.138 BSC	
C	1.400	1.600	0.055	0.063
D	0.170	0.270	0.007	0.011
E	1.350	1.450	0.053	0.057
F	0.170	0.230	0.007	0.009
G	0.500 BASIC		0.020 BASIC	
H	0.050	0.150	0.002	0.006
J	0.090	0.200	0.004	0.008
K	0.500	0.700	0.020	0.028
M	12 °REF		12 °REF	
N	0.090	0.160	0.004	0.006
P	0.250 BASIC		0.010 BASIC	
Q	1°	5°	1°	5°
R	0.150	0.250	0.006	0.010
S	9.000 BSC		0.354 BSC	
S1	4.500 BSC		0.177 BSC	
V	9.000 BSC		0.354 BSC	
V1	4.500 BSC		0.177 BSC	
W	0.200 REF		0.008 REF	
X	1.000 REF		0.039 REF	

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