

The line labelled "JAS" shows Manchester encoding of the NRZI data. The line labelled "MAN" shows Manchester encoding of the NRZ data.

If you look carefully, you may notice that the JAS data is (logically speaking) the result of an exclusive-oring of the clock and NRZI data.

The truth table for an EXCLUSIVE-OR gate is:

Input A	Input B	Output
0	0	0
0	1	1
1	0	1
1	1	0

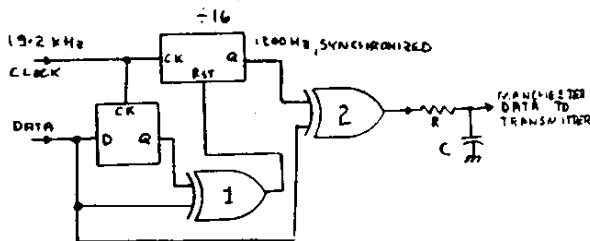
So, all we have to do is take our 1200 baud clock, exclusive-or it with our NRZI data, and apply it to our transmitter.

If you think about the waveform a little more, you will realize that it consists of pieces of square waves that are either 1200 Hz (when 0s or 1s are strung together) or 600 Hz (when 0s and 1s alternate). So, since we have no dc component, and our frequencies of interest are within the passband of a typical FM transmitter's audio response, we can simply shape the digital data itself and transmit it! We don't need any FSK modulators, or tone generators at all!

Of course, there are plenty of sidebands generated at our audio baseband, but by and large we can get the most important ones through our audio system.

Finally, in order to minimize the bandwidth required and meet other requirements of the demodulator, our clock and data must be well synchronized.

Fortunately, the modem disconnect on TNC 1s and TNC 2s provides a signal that can be easily manipulated to provide such a synchronized clock. This is shown schematically below:



The TNC-provided clock of 19.2 kHz is 16 times the desired 1200 Hz clock signal. So, we apply the clock to a divide-by-16 counter and voila! we have our 1200 Hz clock.

Unfortunately, even though the TNC also derives its internal 1200 Hz clock from the same source, the output of our divider has a one in 16 chance of being in the right time relationship to our data, or a 94% chance of being in the wrong phase (before the Murphy factor which guarantees that the phase will be right during prototype testing and wrong when the units are shipped to customers in the field).



This is clearly unacceptable.

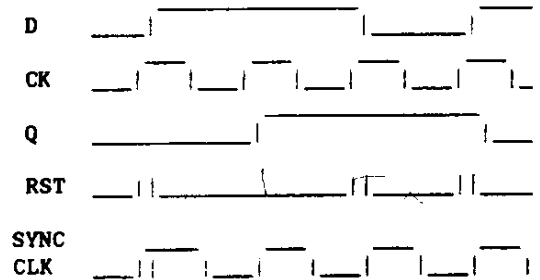
So, we use a D-type flip-flop and an EXCLUSIVE-OR gate to generate a reset pulse to our counter to ensure that it is synchronized with the rising and falling edges of our data.

A "D" flip-flop makes the output line (Q) the same logic level as its input line (D) with every rising edge of the the clock line (CK). When our input data changes state (from a 0 to a 1 or vice versa) the output (Q) and input (D) will be of opposite levels for one clock pulse.



Another way of stating this is that the Q output lags the D input by one clock pulse.

EXCLUSIVE-OR gate 1 compares the D and Q levels. If they are the same, the exclusive-or output is low. If they differ (which happens whenever the data changes between 0 and 1), the output of EXCLUSIVE-OR gate 1 goes high, resetting the divide-by-16 counter at the time of the data change. Thus, the counter output is synchronized to the data. The circuit only requires one data transition to lock the clock to the data.



Next, the synchronized clock is applied to one input of EXCLUSIVE-OR gate 2, with the data applied to the other input. The output is Manchester encoded data suitable for JAS-1.

Finally, the 5-volt square-wave output from EXCLUSIVE-OR gate 2 is attenuated and shaped by filter R1 and C1 to provide a low-level audio signal suitable for application to the microphone input of a transmitter.

There you have it. Simple and cheap!

Next month I hope to get the second installment of the state machine article ready for you. Until then, keep those packets flying!
