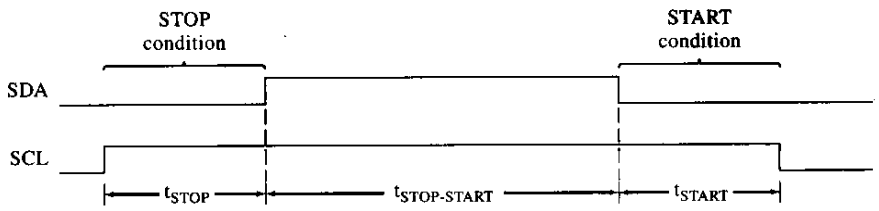
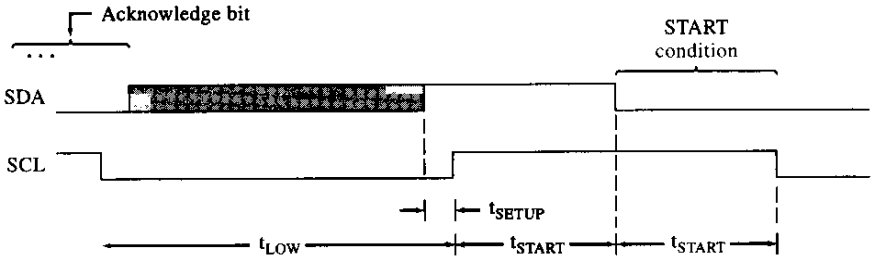
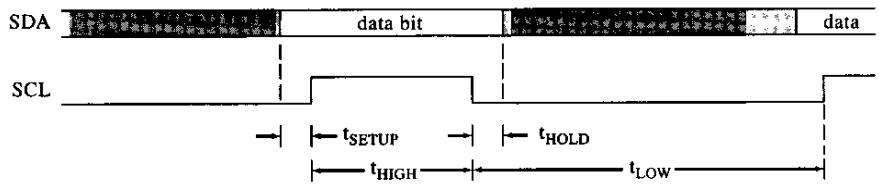


(a) STOP to START constraints



(b) Acknowledge bit to START (restart condition)



(c) Data bit to data bit

Parameter	Constraint	Cycles required to meet constraint		
		OSC = 4MHz Period = 1μs	OSC = 10MHz Period = 0.4μs	OSC = 20MHz Period = 0.2μs
t_{START}	>0.6μs	1	2	3
t_{SETUP}	>0.1μs	1	1	1
t_{HIGH}	>0.6μs	1	2	3
t_{HOLD}	>0μs	1	1	1
t_{LOW}	>1.3μs	2	4	7
t_{STOP}	>0.6μs	1	2	3
$t_{STOP-START}$	>1.3μs	2	4	7

(d) Cycles required

Figure 9-6 I²C bus fast-mode timing constraints.

This use of **FSR** rais

- If these I²C subro tine that also uses
- Any use of indire in conjunction wi

The timing requirem between the instructions on the crystal clock rate. or 20 to insert a number

The equates and vari selected peripheral chip's trol byte. **INTADD** is a **DATAOUT** is used to ho chip by an I²C output su an I²C input subroutine,

The **I2Cout** subrou and calls a **TX** subroutin out on the I²C bus. Fina routine takes the byte p transmits each bit using routine, setting **Z** if ACI

```
delay
```

(a)

(b) Exam

Figure 9