A Simple SDR Receiver

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Abstract:

This article discusses the design and operation of an HF radio receiver operating in the 3.5 to 18 MHz range. The receiver architecture is based on software defined radio techniques and incorporates a Cypress PSoC CY8C3866 component that contains both analog and digital circuits, thus decreasing the receiver's component count.

Key Words:

SDR, software defined radio, PSoC, programmable system-on-chip

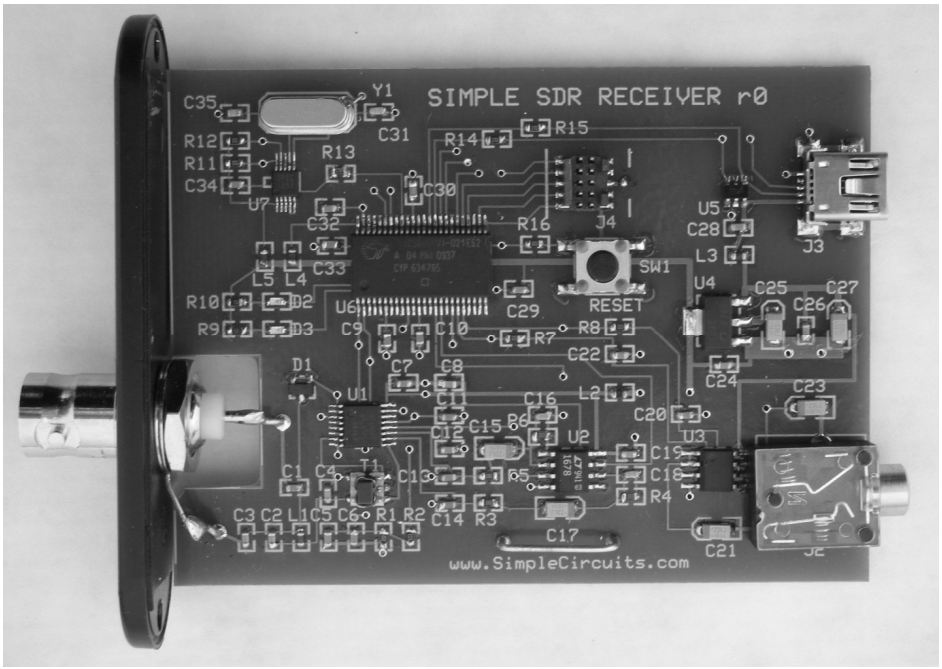

Figure 1: The complete receiver fits on a 3.2 by 2.3 inch printed circuit board.

Background:

Laziness can be an asset for an engineer. Minimizing the number of components in a design decreases the effort of board layout, parts procurement, board construction, and, most importantly, reduces the cost. Being a lazy engineer, I want my designs to have as few of parts as possible, striving for elegantly simple circuits.

During the last few years, I have built a few homebrew receivers using software defined radio (SDR) techniques. Each successive design is simpler, performs better, is less expensive, and uses few components than its predecessor. One of my favorite components to use is the Cypress Semiconductor PSoC series of components. These parts are far more than just a microcomputer; they also contain software configurable analog and digital peripherals on a single chip. Cypress calls the family a PSoC in reference to it being a programmable embedded system-on-chip. The newest series of parts, which Cypress calls the PSoC 3 family, contains a 67 MHz 8051 class microcomputer, an analog to digital converter fast enough and with enough resolution for an SDR receiver, and other valuable functions that are desirable in a receiver design. When I saw this part, I immediately saw its use in an HF receiver.

Receiver design goals:

My goal was to use the PSoC 3 component as the cornerstone of an SDR receiver design. The receiver should be used for casual, conversational listening, not a higher performance receiver for DX use. It should also be built with a minimum number of components, small, and easy to use. I considered adding an LCD display and controls to select the frequency and modes of operations, but decided that the design would have fewer parts and cost less if a PC is used for user input and output. Since the PSoC has a USB port, the receiver can connect to the PC with a USB cable and take power from the PC over the USB cable, saving a power jack, and external power source. Control of the receiver is accomplished by the receiver USB port appearing as a standard com port to the PC. The Ham Radio Deluxe (HRD) program works perfectly to control this receiver.

The basic SDR receiver:

A common SDR receiver is built using a quadrature sampling detector, as shown in the block diagram of figure 2. The quadrature sampling detector is nothing more than a set of analog switches that are enabled and disabled in the particular sequence that samples the input signal four times for each cycle of the desired receive frequency. The four samples represent the 0, 90, 180, and 270 degrees of a sine wave. The output of the detector is amplified by a pair of op amp low-pass filters. After the op amps, the remaining signal processing is performed inside the PSoC microcomputer using digital processing techniques. The processing will digitize the baseband signal, remove the undesired sideband from the received signal, limit the bandwidth of the audio, and then convert the digital samples back into an analog audio signal.

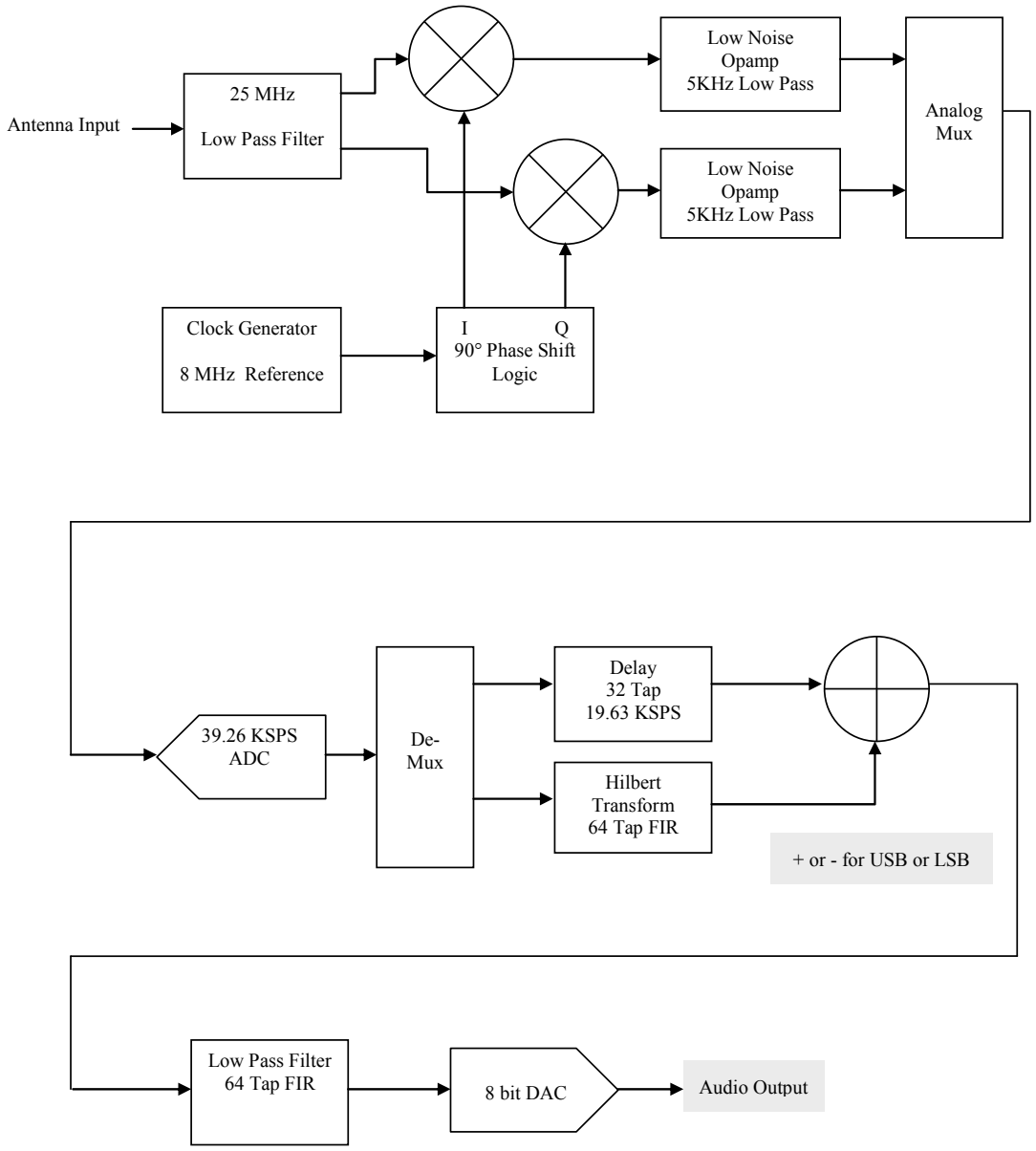

Figure 2: SDR Receiver block diagram.

Circuit Description:

At the antenna input terminals, an RF low pass filter having a 25 MHz corner frequency suppresses signals above the receiver tuning capability. Figure 3 shows the frequency response for the filter.

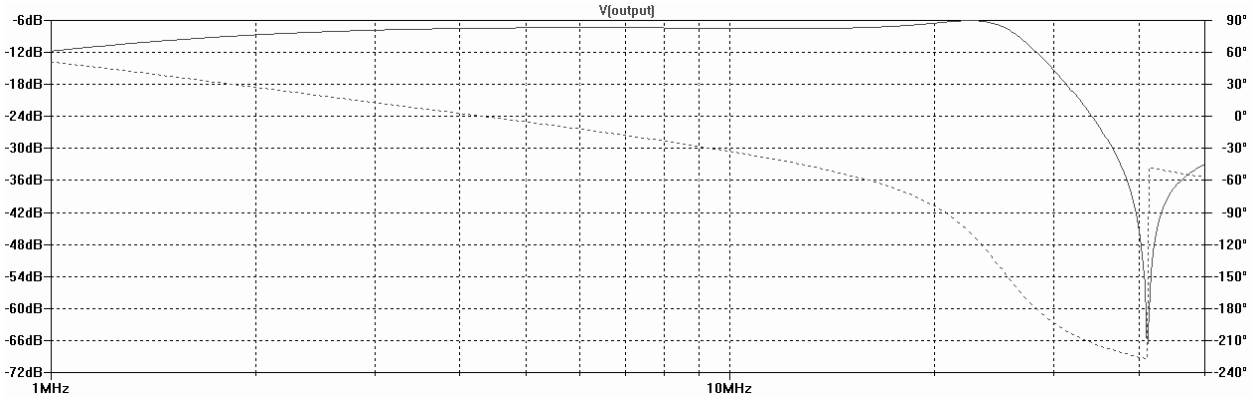

Figure 3: Input RF Filter Response.

Referring to the schematic in figures 6 and 7, U1, a dual 1-of-4 multiplexer/demultiplexer, is used as the sampling detector. This process is similar in functionality as a local mixer, only the control is performed with digital logic switching levels.

A Cirrus Logic clock generator chip, U7, is used to generate a microcomputer controller frequency. It is called a fractional-N clock multiplier and is basically a phase lock loop. The advantages of this component over a discrete digital synthesizer chip (DDS) is that is it cheaper, it has less phase jitter in its output, and it outputs a logic level signal that can be connected directly to the sampling detector multiplexer's control inputs without the need to add a comparator circuit to slice the DDS sine wave output. The clock generator operates at twice the desired receive frequency. The PSoC inputs this clock signal, one rising edge divide by two circuit generates the I clock signal, another falling edge divide-by-two circuit creates the Q clock signal. These two signals are output to the sampling detector multiplexer. They are square waves at the desired receive frequency that are shifted by 90° from one another.

Per the PSoC specification, its inputs are guaranteed to 33 MHz. That means that the clock generator input is the limiting factor in the upper frequency operating range of the receiver. Since this frequency is twice the receive frequency, the highest guaranteed operation is 16.5 MHz. However, after testing several receivers, all have worked to at least 18 MHz (36 MHz clock input) which is near the 17 meter amateur band.

After the mixing process, a pair low noise op amps, U2A and U2B, amplify the base band signals. The part was chosen because of its low noise performance and the ability to operate with inputs and outputs near the ground and power rails. The inputs to the op amps are typically in the microvolt range. Since the op amp circuit voltage gain is on the order of 40 dB at 1 kHz, the output signals are on the order of a few hundred microvolts to a few millivolts. This circuit includes a first order low-pass filter having a 3 kHz corner frequency. It is important to reduce the frequencies above half of the analog to digital converter sampling rate which is called the Nyquist frequency. Otherwise, images will appear at frequencies near the sampling rate. Figure 4 shows the frequency response of the op amp circuit.

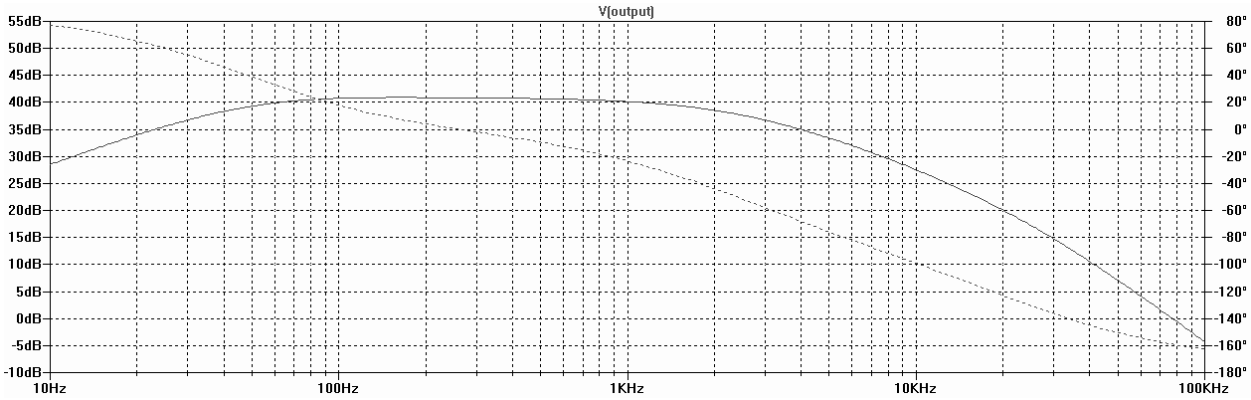

Figure 4: Op amp circuit frequency response.

From this point, all of the signal processing is performed in the digital domain, and, specifically, inside the PSoC, U6.

The PSoC has a single analog to digital converter (ADC). Since there are two base band signals to process, the I and the Q channels, an analog multiplexer is used to switch one of the two inputs to the ADC input. It is desirable to have a high sample rate and a high number of bits, but the best tradeoff I could find is to use the ADC in a 14 bit mode and sampling at 39,260 samples per second. Since a sample from each input channel is necessary, the equivalent sample rate per channel is 19,630 samples per second. Therefore, the Nyquist frequency is almost 10 kHz. The op amp frequency response at 10 kHz is about 15 dB below the desired passband. This is not great, but leaves room for improvement in a future version.

The rest is all digital processing. The PSoC 3 family of parts have an interesting internal hardware feature they call a digital filter block, or DFB, and it consists of a 24-bit fixed point, programmable limited scope DSP engine. This is a dedicated hardware accelerator block that operates independently of the main 8051 processor. It consists of a dedicated multiplier and accumulator that calculates a 24-bit by 24-bit multiply 48-bit accumulates in one system clock cycle. It is optimized to implement a direct form Finite Impulse Response (FIR) filter that approaches a computation rate of one FIR tap for each clock cycle. This block is used as two independent, 64 tap, digital filters.

Alternating outputs from the ADC are loaded into either a 32 sample long delay line or one of the two digital filters. This digital filter uses a set of coefficients that form an all-pass filter having a flat magnitude response, but phase shifts all frequency in its passband by 90°. This is called a Hilbert filter. Suppressing either the upper or lower sideband is accomplished by phase shifting the Q channel baseband data and either subtracting or adding the filter output to the delayed I channel baseband data. The delay is necessary to compensate only for the delays incurred by the processing of the Hilbert filter. The output of the addition is one of the two sidebands.

After the removal of the undesired sideband, the data stream is feed into the other half of the PSoC digital filter block configured as a low-pass filter. This filter has a steep rolloff as shown in the figure 5 for a 2 kHz filter. This is the advantage of processing in the digital domain as compared to a set of analog filters. Steep rolloffs and repeatability of the filter performance over wide temperature ranges and from part to part variations are the reasons to use digital processing.

The output of the low-pass filter is fed into one of the PSoC's 8 bit digital to analog converters (DAC) that converts the data stream back into an analog signal. This signal is buffered with a unity gain op amp, U3, and passed to the output connector.

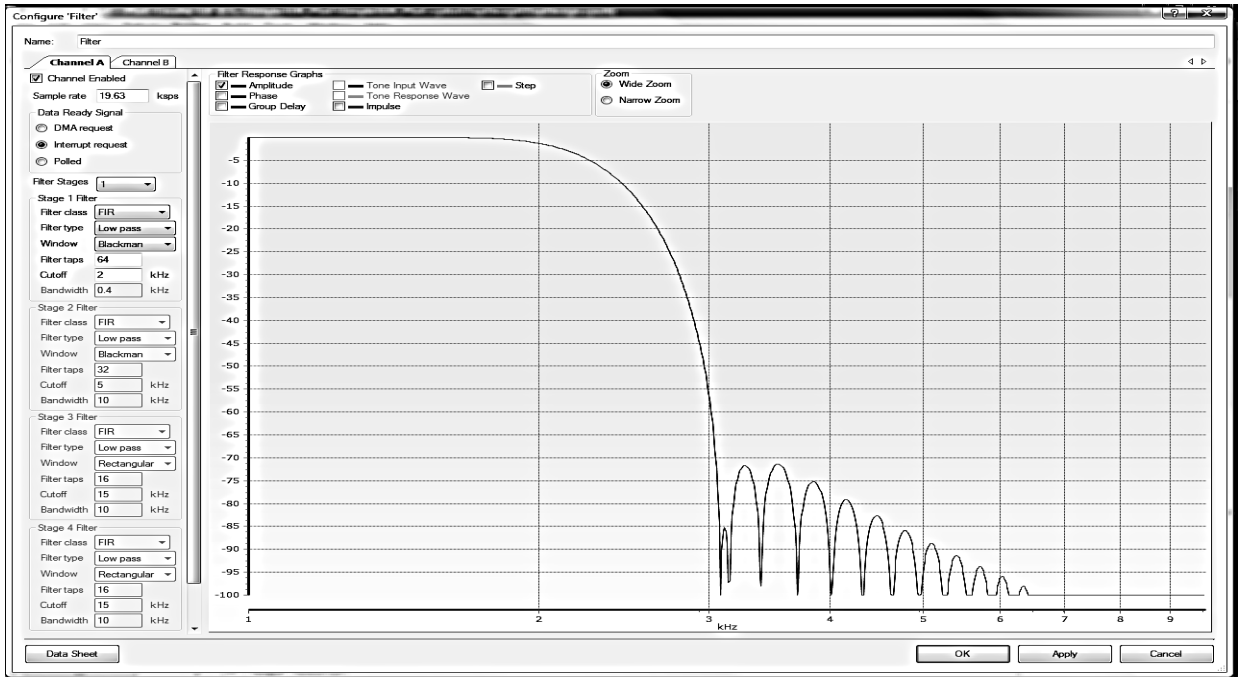

Figure 5: PSoC Digital low-pass filter response.

Operation:

The PSoC has an internal USB full speed port. I wrote firmware for this device to implement a serial communication port. When connected to a personal computer, the receiver will look like a serial device. Using the standard CDC (communication) drivers that are built into Windows, the receiver can communicate with Ham Radio Deluxe. The receiver firmware uses the Elecraft K2 communication protocol. I chose this protocol because it was one of the few that I could find that had a written specification available.

The receiver's audio output will directly drive low impedance headsets. The use of good computer speakers that have a built-in amplifier and volume adjustment is ideal. There is no volume control capability in the receiver. Headsets need their own volume adjustments.

The radio works on all frequencies from 3.5 MHz to at least 18 MHz (80 to 17 meters).

Any one of 4 different receive filter bandwidths can be selected using HRD. FL1 is a 2.5 KHz low pass filter, FL2 is a 2.0 KHz low pass filter, FL3 is a 1.5 KHz low pass filter, and FL4 is used for CW and RTTY and is a 1.0 KHz band pass filter that is 400 Hz wide (+/- 200 Hz).

The attenuator button (ATT) will turn decrease the volume by several dB.

Performance:

The minimum discernible signal (MDS) is approximately -117 dBm. A typical receiver would normally be more towards the -120 dBm number. However, on the lower HF frequencies, where atmospheric and man-made noise dominates, the performance is sufficient. In fact, in a head to head comparison with my Flex Radio Flex-3000, I find it difficult to hear any difference. Not bad for a $50 receiver.

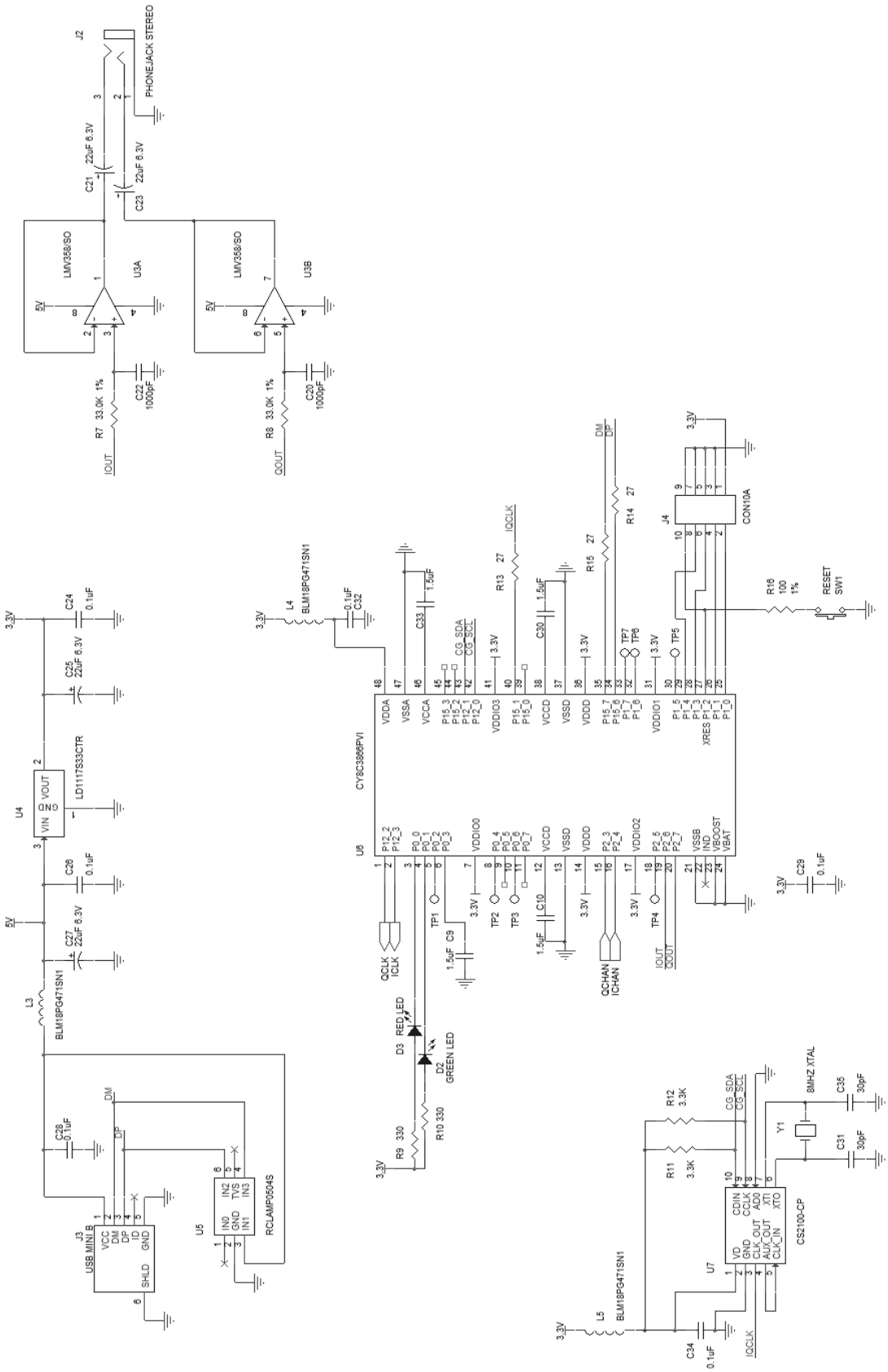

Figure 6: SDR Receiver schematic, sheet 1, digital.

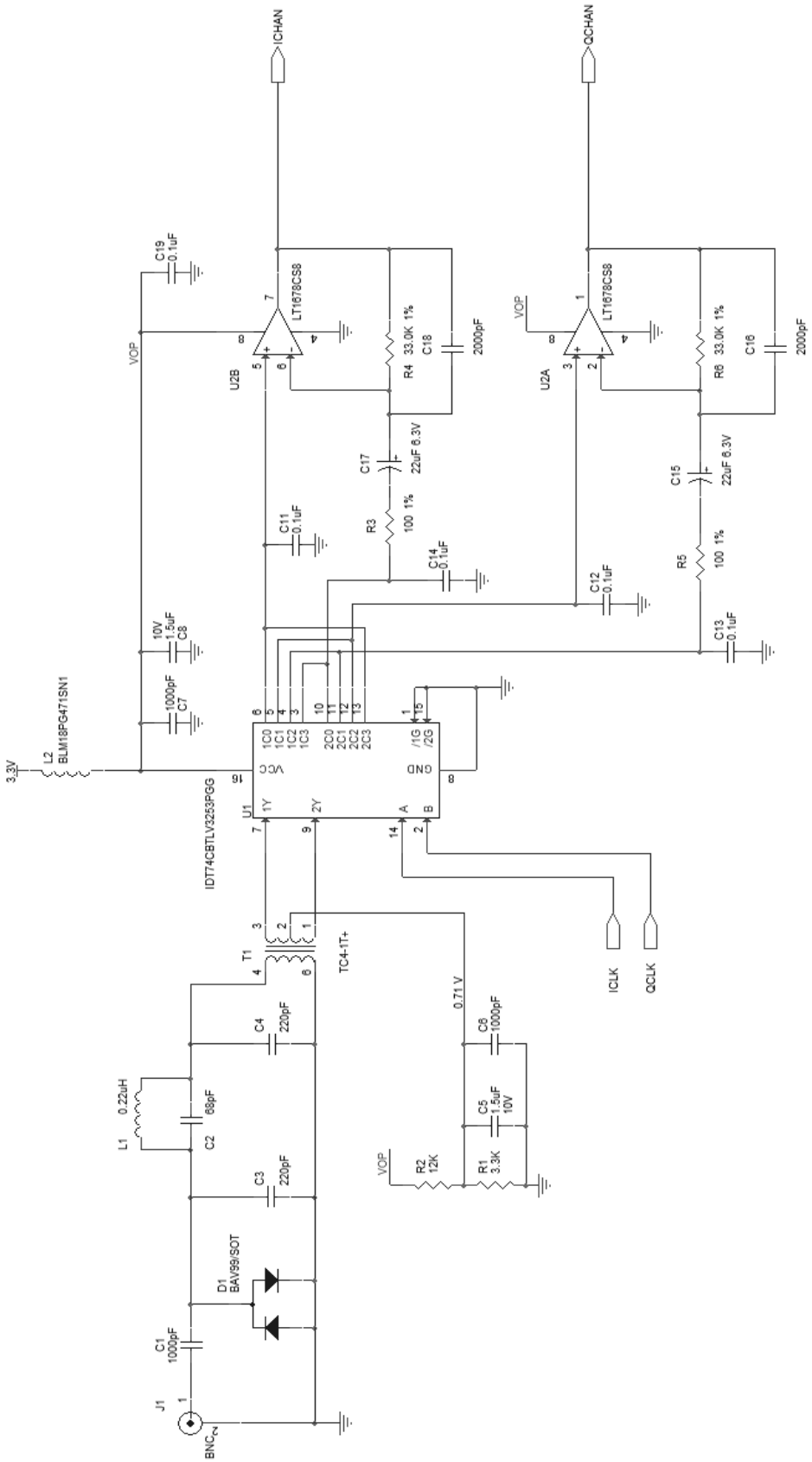

Figure 7: SDR Receiver schematic, sheet 2, RF.