Project Design for TAPR Manufacturing

Design for Manufacturability

-or-

How to ease your project into mass production with the least amount of pain

(both yours and TAPR's)

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Who Cares About This?

Anyone who…

- Wants to build more than one or two
- Wants these many copies to actually work
- Make the best use of limited manufacturing resources

Because…

- One on your bench that doesn't work is a "Project"
- 500 in inventory that don't work is a nightmare
- Poor use of resources might mean it never gets built

Process Yields Results

We follow a process because it…

- Reduces time to market
- Eliminates errors
- Increases the manufacturing yield
- Increases the probability of success

Process Yields Results

We follow a process because it…

- Reduces time to market ***(FASTER)***
- Eliminates errors ***(BETTER)***
- Increases the manufacturing yield ***(CHEAPER)***
- Increases the probability of success ***(SURVIVAL)***

Process Yields Results

And Because we want the following benefits:

- Lower the total cost of production
- Get many boards in people's hands
- Advance the state of the art (especially with OHL)
- Have ***fun*** in the process!!!

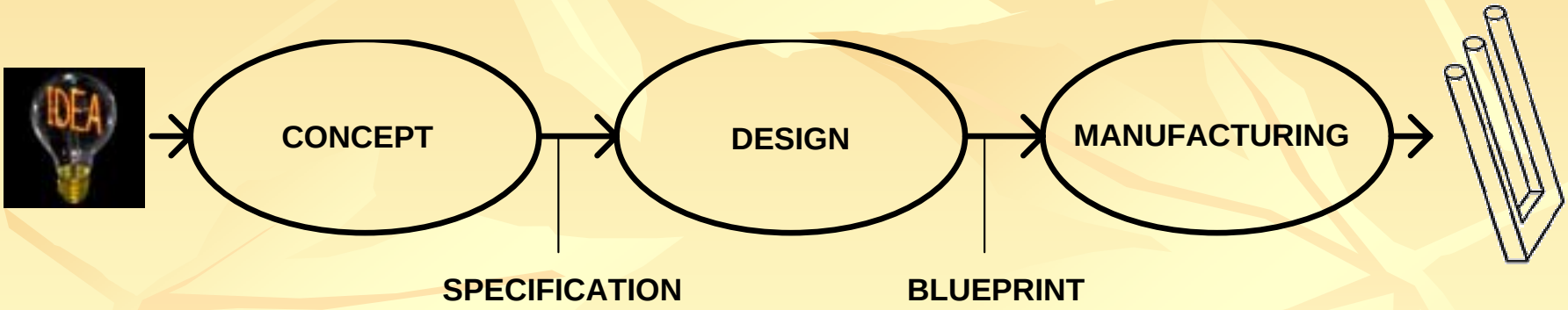
Process Yields Results

Not all Process is created equal…

We want ***GOOD*** Process

Project Flow Trinity

Project flow through the three phases from idea to the shelf



Process *becomes more important* as we move to the right

Concept Phase

Concept stage input: Initial Idea

- Discussion/peer review
- Experimentation (use modified existing boards)
- Proof of concept
- Partial or sectional prototype (use evaluation boards)
- Formalization of assumptions and functionality
- Final peer review
- Very iterative

Concept stage output: Product Specification

Design Phase

Design stage input: Product Specification

- Hardware design (schematic capture)
- Peer review
- PCB design (layout and routing) and review (not peer)
- Prototype (Alpha) build
- Design validation (extensive testing)
- Iterative, typically 2 to 3 diminishing cycles

Design stage output: Gerber, BOM, schematic files

Manufacturing Phase

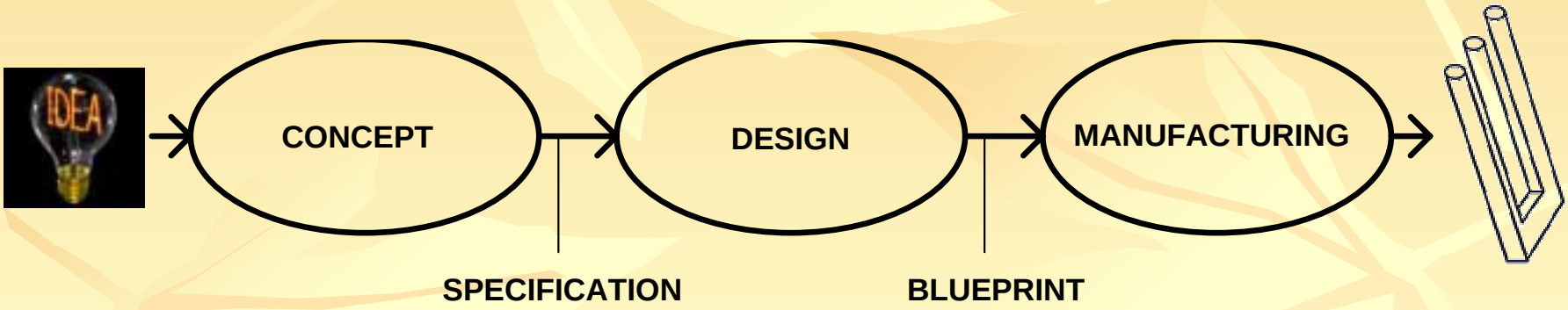
Manufacturing stage input: Gerber, BOM, schematic files

- Cost out BOM, determine parts availability, set sale price
- Assemble documentation package
- Schedule assembly
- Procure parts and PCB (may also require scheduling)
- Assemble and inspect PCBs (by machine and by hand)
- Develop test procedure and build test fixture
- Final inspect, program, test, bulk package for shipment

Manufacturing stage output: Built and tested product

Project Flow Trinity

Project flow through the three phases from idea to the shelf



The more complete and accurate the Blueprint, the easier the transition to the Manufacturing Phase will be

Blueprint Trinity

1. Schematic/Netlist
2. Bill-of-Material (BOM)
3. Layout (Gerber) data

Schematic *is* the Design!

- Use a standard schematic tool
- Follow simple schematic rules
- Draw the schematic simply, clearly and uncluttered
- Include ***all*** part information in the schematic
- Include ***some*** layout information in the schematic
- Create a Fab Notes document to ease PCB fabrication

Standard Schematic Tools

- Cadence OrCAD Capture (Windows)
  - $1500+ per seat
  - AMSAT has shared OrCAD licenses available free to developers
- KiCAD (Linux, Windows)
  - Open source (GPL), free license
- gEDA (Linux)
  - Open Source (GPL), free license
- CadSoft Eagle (Linux, Widows, Mac)
  - $50 (light) - $250 (std) - $500 (pro)

Simple Schematic Rules

- Only one off-page connector for each unique signal per page
- Off-page connectors should be at sheet edges, not buried within sheet
- Off-page connectors should indicate signal direction, if possible
- Use inter-sheet references on all off-page connectors, if possible

Draw Simply and Clearly

- All instances of a signal on the same page must connect with a wire
- Use more and/or larger sheets
- Use a page size no more than one size bigger than your printable size
  - Typically “C” for a “B” size printer or “B” for a letter-size printer

A=8.5”x11”, B=11”x17”, C=17”x22”, D=22”x34”, E=34”x44”

Include Part Information

- Reference designator (R3, C6, U10)
- Part value (10K, 22uF, EP3C40)
- Part manufacturer (Rohm, AVX, Altera)
- Manufacturer part number (EP3C40Q240C8N)
- Vendor (Digi-Key, Mouser, Arrow)
- Vendor part number (544-2551-ND)
- PCB footprint (0603, EIA-B, PQFP240)

Include *More* Part Information

- Capacitors
  - voltage
  - tolerance
  - dielectric type/temperature coefficient
- Resistors
  - power
  - type, if special
- Toroids
  - Don't use toroids
- Other parts
  - whatever ratings are critical to the design

BOM Formatting

- Group parts:
  - One line per part type
  - ***NOT*** one line per reference designator
- Include part data
  - manufacturer and manufacturer part number
  - vendor and vendor part number
- Include package type and/or size
- Additional fields (tolerance, power, etc) needed on schematic only

Optional Parts

Why Do This?

- Manufacturing variants
- Optional functionality
- Test and/or debug circuitry
- Future cost reduction

Optional Parts

- Optional parts should contain *all* part data fields
- Add “DNI-” prefix to part value field
- e.g., “10K” becomes “DNI-10K”
- Note that “DNI” now appears in both BOM and Schematic

Include Layout Information

- PCB footprint (obviously)
- Flag critical nets with text notes in schematic
  - Power, timing, termination, routing
- Group components
  - by circuit function (add notes for proximity information)
  - by physical proximity in layout
- Switch and Jumper functions
  - Jumper settings are especially helpful
  - Labels for silk screen (SS_DESC property)

Check for Common Errors

Schematic → Netlist Checking

- Check for netlist errors *before* going to layout
- Automatic schematic checking
  - Run DRC from your schematic tool
- Manual checking
  - Duplicate and/or shorted power buses (“5.0V” ≠ “5V”)
  - Similar, but not identical, net names (“data-in” ≠ “data_in”)
  - Single node nets (DRC normally catches this)

Check for Common Errors

Layout (Gerber File) Checking

- Automatic Gerber file checking
  - Run DRC from your layout tool
  - Many PCB shops provide free on-line DRC service
- Manual Checking
  - Check ***EVERY*** polarized component (LEDs, caps, Zeners, etc)
  - Check ***EVERY*** connector and header for proper pin 1 orientation
  - Check ***EVERY*** connector for proper pin order (reverse/mirror)
  - Check ***EVERY*** plane layer (many are placed manually)
  - Double check ***EVERY*** power connector for proper polarity

Check for Common Errors

Layout (Gerber File) Checking, cont'd

- PDF files are useful, but…
- Free Gerber viewers are readily available (Win and Linux)
  - GC Prevue is standard
  - list of others here:

    http://www.mitsi.com/PCB/free%20viewers.htm
- Note that layout errors may not show up on the schematic
  - Silk screen data is almost always generated manually
  - An incorrect silk screen can cause assembly errors

Create Fabrication Notes

- PCB material (FR4)
- Copper thickness (1 oz/ft^2)
- Layer stack up (order)
- PCB dimensions (100mm x 120mm)
- Designer contact info

Sample Fab Notes File

PCB Material FR4, thickness 0.062" nominal, 1 ounce copper, 4 layers, white silkscreen, green soldermask. There is no gold plating, unless otherwise required.

Stackup order: SST, SMT, TOP, PWR, GND, BOT, SMB, SSB.

Datum is the lower left corner of the PCB as shown in the drawing above. The provided Gerber and Excellon files share this same datum.

⏃ This symbol represents the approximate break-off tab locations if the boards are panelized.

There are two (2) non plated holes 0.116" diameter at coordinates (0.215, 0.110) and

Summary

To release to manufacturing, you need:

- At least three fully tested Alpha PCBs
- Fully annotated schematic
- Complete BOM (no TBDs or missing part data)
- Gerber files
- Clean DRC on schematic and Gerber files
- Fab Notes file

TAPR Can Help With Funds

Because

- You put in your time and expertise
- Community peer reviews give early feedback
- Hardware is expensive

Designers should not have to both bear the cost *and* donate their time

Thank you!

Kit Information At:

www.tapr.org