Clocking the Data

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ABSTRACT

Many oscillators attached to the microprocessors and microcontrollers today are simply inverter stages intended to become Pierce-style oscillators. There are still many options and design considerations to make when attaching components onto the device to attain the desired results.

INTRODUCTION

Issues surrounding clock oscillators and their design include frequency, frequency stability, startup time, and overtone responses. Understanding these issues and how they are manifested in the circuit design will help minimize problems related to clocking.

KEY WORDS

Negative Resistance: An index indicating the gain of an oscillator stage at the time of startup of the oscillator.

Gain Margin: A ratio of the absolute value of the negative resistance to the ESR of the crystal.

Crystal ESR: The equivalent series resistance of the crystal at resonance.

Overtone: The near odd multiple resonances of the crystal.

OSCILLATOR DESIGN

When designing the oscillator, there are two criteria. We need gain, and we need phase shifting to take place. We can look at the inverter stage as the element with the gain (more than 1) and the loading capacitors as the phase shifters (along with the gate delay and the inverter shift).

CIRCUIT DESIGN:

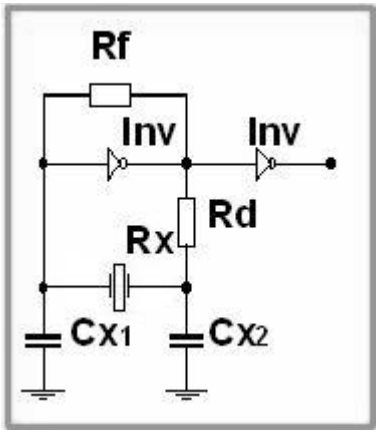

Figure 1. Pierce inverter circuit

What are all these components and what are they there for [1]? Typically, the inverters are internal to the IC being used. There is a buffer inverter that follows the oscillator inverter. Most of the time, the IC manufacturer includes a feedback resistance that pulls the inverter into a medium bias for proper operation. If the feedback resistance is not within the IC, then this must be added externally for biasing.

CX1 and CX2 are the loading capacitors. These provide a phase shift that will setup the oscillator to oscillate on frequency. If we view the grounds as a wire that runs from one capacitor to another, we will see that the two capacitors are in series with respect to the crystal. Therefore the series equivalent of these two capacitors is a part of the loading capacitance. Other load capacitance values come from stray capacitance from the PCB design, crystal shunt capacitance, and inherent I/O capacitance on the IC being used. [4] Ideally, these load capacitances account for 180 degree phase shifting that takes place for proper circuit oscillation. This compliments the 180 degrees phase shifting of the inverter stage. Ideally, when the capacitive loads shunted with the crystal are added up, they should equal the manufacturer's equivalent capacitance so that it will be on frequency.

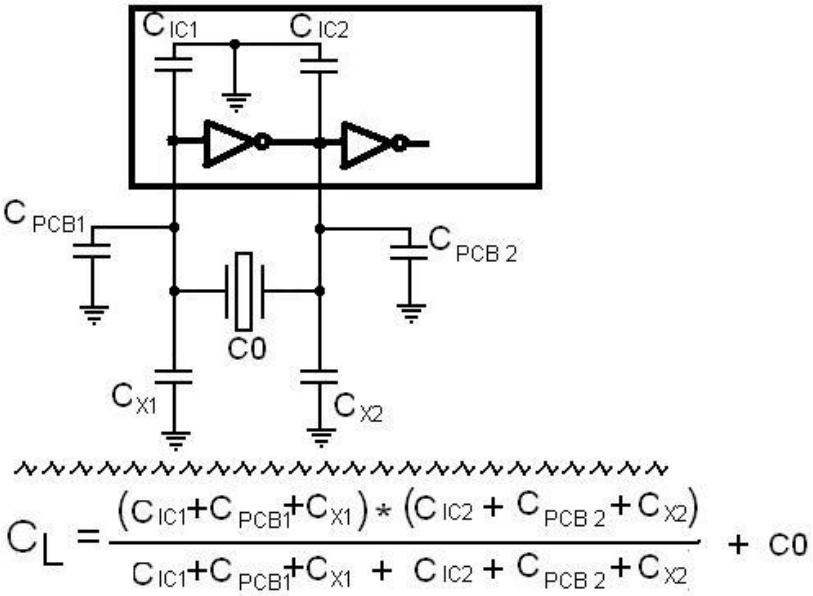

Figure 2 *Showing the excess stray capacitance that adds to crystal loading.*

The dumping resistor, Rd, is a resistor that can be used to reduce the gain of the oscillator circuit at overtone frequencies. [1] Rd and Cx2 will create a first order filter that will lower the bandwidth of the oscillator stage. This is helpful in minimizing overtone responses. At the same time, it can be used to reduce the drive and negative resistance of the oscillator.

Overtones should never be confused with harmonics. Harmonics are signal outputs derived from the amplitude distortions of the fundamental. Overtones are crystal resonances roughly related to only the odd order multiples of the fundamental.

The foremost consideration to make when designing the crystal clock oscillator is selecting the crystal. The crystal is the device with the characteristics of a very precise series-tuned tank circuit.

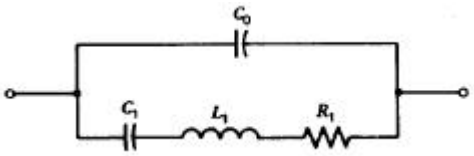

Figure 3. *Equivalent discreet component schematic.*

In Figure 3, we see the schematic of the crystal as it will operate in your circuit. Let's go over the different component values and what they mean to you. [2]

C1 – Motional Capacitance. This is the capacitance value in the series tank circuit that the feedback path in the oscillator circuit will see. This value, although usually very tiny, is very important to understand because this value will help determine the Q of the crystal. These values are typically in the tens of femto Farads.
L1 – Motional Inductance. This value works directly with the Motional Capacitance value to determine the resonate frequency for this crystal. The frequency formula works for these two values to determine the oscillation frequency. These values are typically in the tens of milli Henries.

$$f = \frac{1}{2\pi\sqrt{L \cdot C}}$$

Eq 1. *Frequency Formula*

Where f is the resonate frequency in Hz, L is the motional inductance in Henries, and C is the Motional Capacitance in Farads.

R1 – Motional Resistance. This is the resistive value that the circuit will see when the crystal is operating at resonance. At resonance, the impedance values of the series capacitance and series inductance will cancel, leaving only the motional resistance to be seen in this leg of the circuit. These values are typically from a few ohms to under 100 ohms. KHz crystals (tuning fork) will be in the 10k region.

C0 – Shunt Capacitance. When the electrodes are placed onto the crystal blank, the parallel surfaces of these platings create a shunt capacitance across the crystal. This looks like a load to the crystal circuit in the circuit design. If there is frequency tuning planned for this circuit, it is usually preferred that this

value be kept as small as possible to keep from swamping out the tuning capability. These values usually range from 0.2 pF to 6.0 pF depending on the crystal design.

LOADING THE CRYSTAL.

There is talk of a series resonate and a parallel resonate crystal. These are NOT different types of crystals, but rather a different way they are defined. The series resonate frequency will always be lower than the parallel resonant frequency. Always ask for a parallel crystal and give the desired load capacitance for the desired operating frequency. Typically ~12 pF.

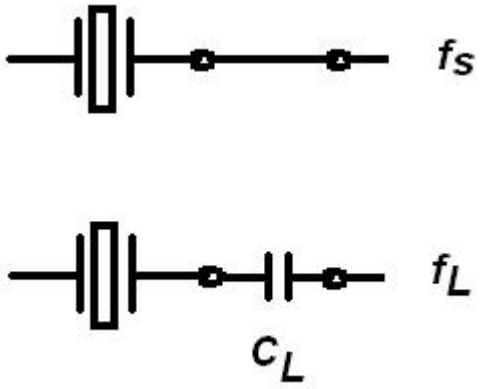

Figure 4. *The fs represents the series resonate and fL represents the parallel resonate. fL has the capacitive load attached.*

When the crystal is designed, consideration is made as to what the load capacitance will be, and the crystal is designed to operate at the desired frequency with that capacitive load considered. Therefore, we only really consider the parallel resonate crystal when ordering the crystal.

NEGATIVE RESISTANCE:

Negative resistance is the measurement of the oscillator startup properties. Usually, startup takes place in under 10 milliseconds, so it is difficult to see what is going on in such a short period of time. Therefore, we can quantify negative resistance by breaking the trace to the crystal and installing a resistor in series. When we do this, we can see the maximum resistance that will allow for an oscillation. This gives us a good indication as to what the "negative resistance" of the oscillator actually is. The best results will be over 1k ohm.

GAIN MARGIN:

Taking the negative resistance and dividing by the crystal resistance, we find the "gain margin". If we measured a negative resistance of 1k ohm and we know our crystal has no more than a 30 ohm resistance, we have a gain margin of over 30 and we know that this margin will remain very reliable. In fact, gain margins of 10 are satisfactory for most microprocessor applications.

$$Gain\ Margin = \frac{|\ Negative\ Resistance\ |}{Crystal\ ESR}$$

Eq 2. Gain Margin

DRIVE LEVEL:

Since crystals have a crystal resistance, they are limited by the power that they can dissipate. Many crystals will operate well in the 100 micro watt region. This measurement is difficult to measure. We can calculate to estimate the crystal power.

$$P \approx \frac{1}{2}(2\pi \times f_{loaded} \times C_L \times V)^2 \times Rs$$

Eq 3. Crystal Power [3]

Where f_{LOADED} is the loaded frequency of the crystal, CL is the load capacitance, V is the voltage across the crystal and RS is the ESR of the crystal. This value will be more accurate if it is in RMS.

OVERTONES:

Usually, with a well designed crystal, there are little concerns of overtone operation with most crystals. But there is a possibility that the circuit can take off on the overtone frequency and operate at the undesired mode. If there is a resistor inserted in the circuit (as an Rd) we can minimize the gain at the higher frequencies and possibly eliminate any opportunity for an overtone oscillator response. Remember in the Barkhausen Criteria that there needs to be a gain of over "1". If the overtone gain margin is less than "1" there will be no possibility of an oscillation taking place at the overtone frequency.

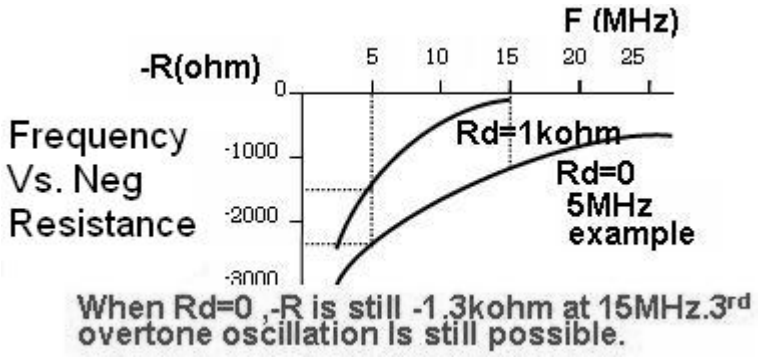

Figure 5. *Oscillator stage over frequency using Rd = 0 and Rd = 1k.*

Taking a hypothetical situation as in figure 5 and our crystal resistance at the third OT of 15 MHz is 500 ohms, then there will be ample negative resistance for the overtone frequency when the Rd is equal to 0 ohms. In this case, using a 1k ohm resistor for Rd, the 15MHz response drops to only a few ohms negative resistance. [1] Therefore, it cannot oscillate in this instance on the overtone frequency. We still have plenty of negative resistance for the fundamental.

CONCLUSION

Oftentimes, we can throw components together in the Pierce oscillator and we can make it operate, but issues of crystal power dissipation, crystal loading, and the possibility of overtone responses, to name a few, can disrupt proper operation of the digital circuit in the future if these design considerations are ignored. We prefer a crystal that is not getting over driven and a circuit properly loaded for nominal frequency operation.

REFERENCES

[1] Benjamin Parzen, Arthur Ballato (1983) Design of Crystal and Other Harmonic Oscillators – pp 386, 393

[2] WH Hayward (1982) Introduction to Radio Frequency Design – pp 287 – 288

[3] Chrontel (2001) AN-06 Crystal Oscillator Application Notes – pp 2 – 3

[4] Kyocera (2006) For Proper Use of Crystal Units – p 6