A 9600 Baud modem for the LPT port

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Introduction

The 9600 Baud FSK modulation according to G3RUH uses our limited bandwidth ressources much more efficiently than the popular 1200 Baud AFSK. But one reason for the packet user not to switch to FSK is the higher price of the modem hardware - usually a TNC2 clone with a large FSK modem board. In contrast, 1200 Baud AFSK can be decoded with a very simple and cheap adapter to a PCs COM port containing not much more than a TCM3105, and originally designed by Johannes DG3RBU (BayCom). Packet decoding is done by software in the PC, and there is a wide variety of drivers. Even the power supply is derived from the COM port.

We present here a simple modem for 9600 Baud FSK which can be connected to a LPT port (provided its IRQ is installed). It is also powered from the port and does not need any alignment. Several drivers for DOS [1] and LinuX are available because of its compatibility to the BayCom PAR96 modem (and its PacComm clones). With DOS and the BayCom program it operates with any computer higher than a 10 MHz 286. It has been originally published in [2].

Hardware description

Fig. 1 shows the circuit diagram. The key to the high functionality with few parts is the use of a microcontroller from Arizona Microchip, the PIC16C84 [3]. This IC contains a complete microprocessor system which can operate from a 2V/1mA power supply. A dual CMOS shift register is used to decouple the time-critical data transfer to the host PC, and a quad opamp provides all necessary analogue filtering including the threshold comparator function. The Analog Devices OP491 is a micropower opamp with medium speed and rail-to-rail capability down to 2.7 V single supply. The analog circuit is equivalent to other FSK modems, thus preserving the high signal purity.

The complete circuit is supplied via 3 data lines from the interface. Any typical LPT port output is similar to at least a LS-TTL output and can drive few mA against 3.3 V. Desktop PCs usually have a lot more power in the LPT to drive long shielded printer lines with high speed. The modem has been tested with a variety of notebooks and desktops, and the internal modem supply never fell below 3.0 V.

Microcontroller internals

The processor is always running in one of two software loops with a length of exactly 96 command cycles, one for receive and one for transmit operation. Because one command cycle uses 4 clock cycles this is just one bit period of a 9600 Baud signal. Both loops are written such that the execution time is independent of all branches and subroutine calls. No interrupt or timer is used in order to maximize execution speed.

During transmit most time is used for the calculation of the output samples which is done 4 times per bit length. The 8 stage FIR filter response on a bit stream is stored in two tables, and combined by the PIC in real time in order to save ROM space. One single table would require 256x4= lk byte (8 bit length, 4 times oversampling) which exceeds the limits of the 16C84. By using two tables, where the response is separated into two 4-step parts, only 2x16x4= 128 bytes are required. The calculated sample is then output on a 7 bit wide port and D/A converted by a metal film resistor array.

During receive the threshold comparator output is sampled four times per bit. These binary samples are the only input to the decoder. First the clock is regenerated by a smart DPLL with a fast lock time but a smooth track as long as DCD is active. The DPLL is realized by incrementing or decrementing the code loop by one NOP - the whole software runs behind the input signal. Then the correct sample per period is used for demodulation. DCD is generated from the 4 samples which characterize the position of the input zero crossings. The derived raw DCD information is averaged over 50... 100 periods for a reliable DCD operation. Scrambling and bit stuffing are done in the PC driver, according to the original BayCom PAR96, to maintain compatibility.

The PC interface

Every 16th bit of the HDLC data stream the PICPAR modem generates an interrupt via pin 10 of the LPT. The PC responds to this interrupt and inputs or outputs 16 bit of data via pin 2/12 with the clock coming from the PC at pin 4. This burst data transfer minimizes the interrupt load and allows operation even with moderate speed PCs. The data is stored in a 16 stage shift register and then transfered serially again to (or from) the PIC - this time the clock comes from the PIC to match with its close real time HDLC port operation. DCD and PTT are connected statically via extra lines.

Construction

The prototypes have been built on a two layer PCB of about 2.5 x 3.7 sq. inch. This version is shown in the Figures 2 and 3. The component density is low, and there are only few tracks on the component side of the board. The board layout is public domain for noncommercial use in amateur radio and can be obtained from one of the authors (df9ic) as HP/GL or PCL. The processor firmware will not be disclosed but programmed processors are available from [4]; also complete modems based on this design, as kits and finished modules. Especially attractive is a very small SMD version which fits into a D shell adapter case.

References

[1] PC/FlexNet, a modular packet radio software package from Gunter Jost DK7WJ.

[2] Rech, W.-H., DF9IC: Einfache Modems mit PIC-Prozessoren (simple modems with PIC processors). Proceedings of the 12th International Packet Radio Conference Darmstadt 1996, 7-17. (in German)

[3] PIC 16/17 Microcontroller Data Book. Microchip Technology Inc, 1995.

[4] BayCom GmbH, Bert-Brecht-Weg 28, D-30890 Barsinghausen, Germany. e-mail: kneip @ mst.uni-hannover.de.

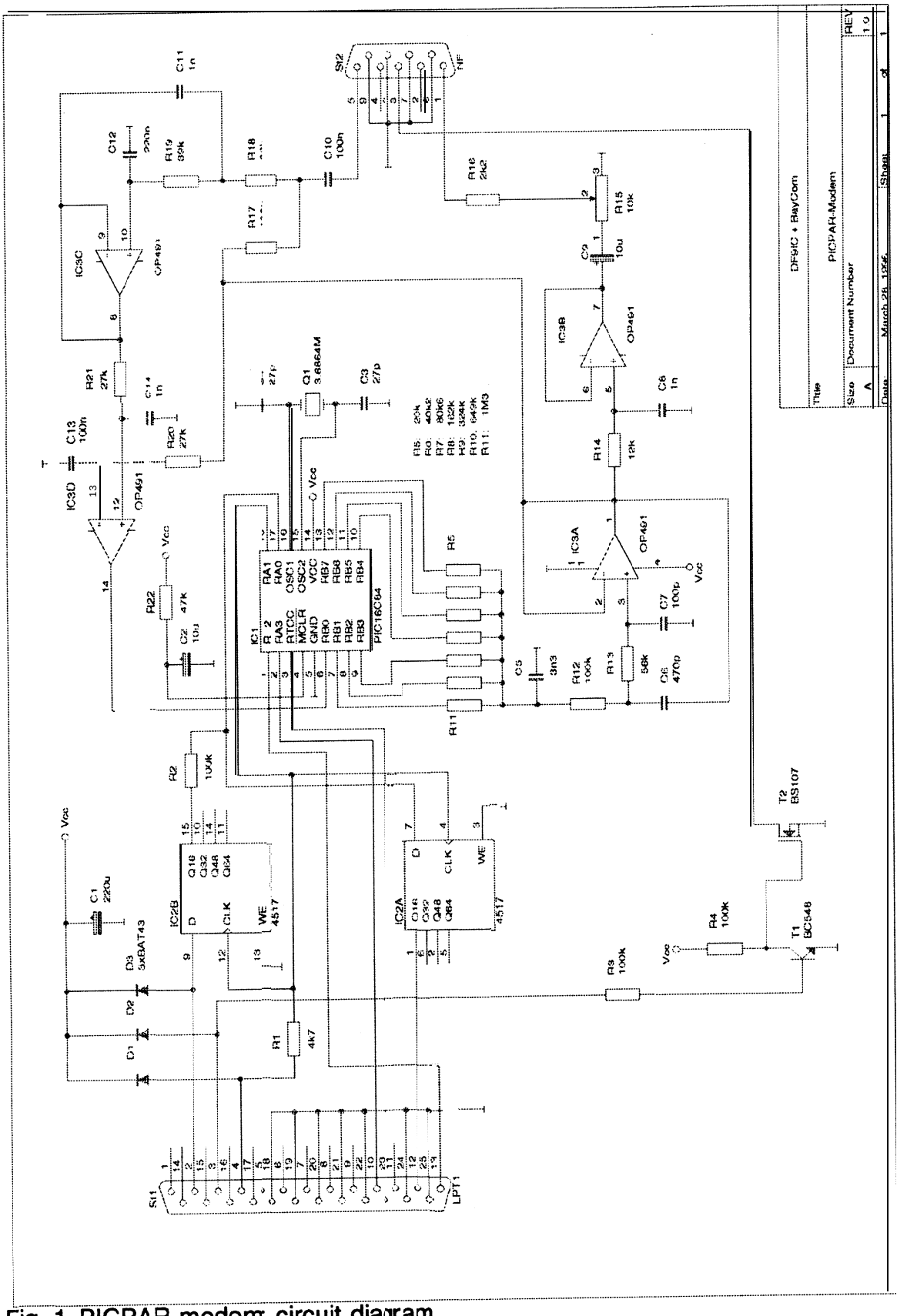

Fig. 1 PICPAR modem circuit diagram

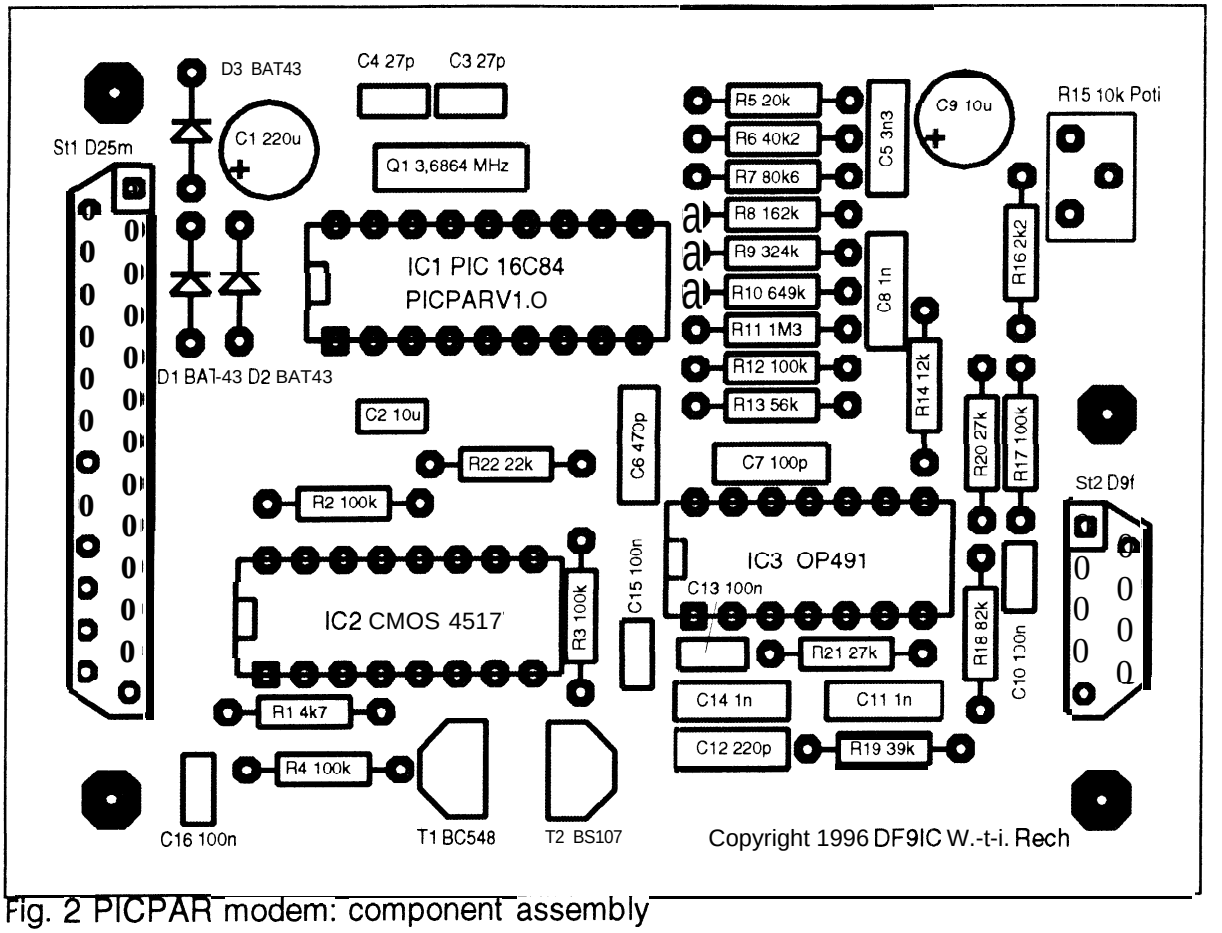

Fig. 2 PICPAR modem: component assembly

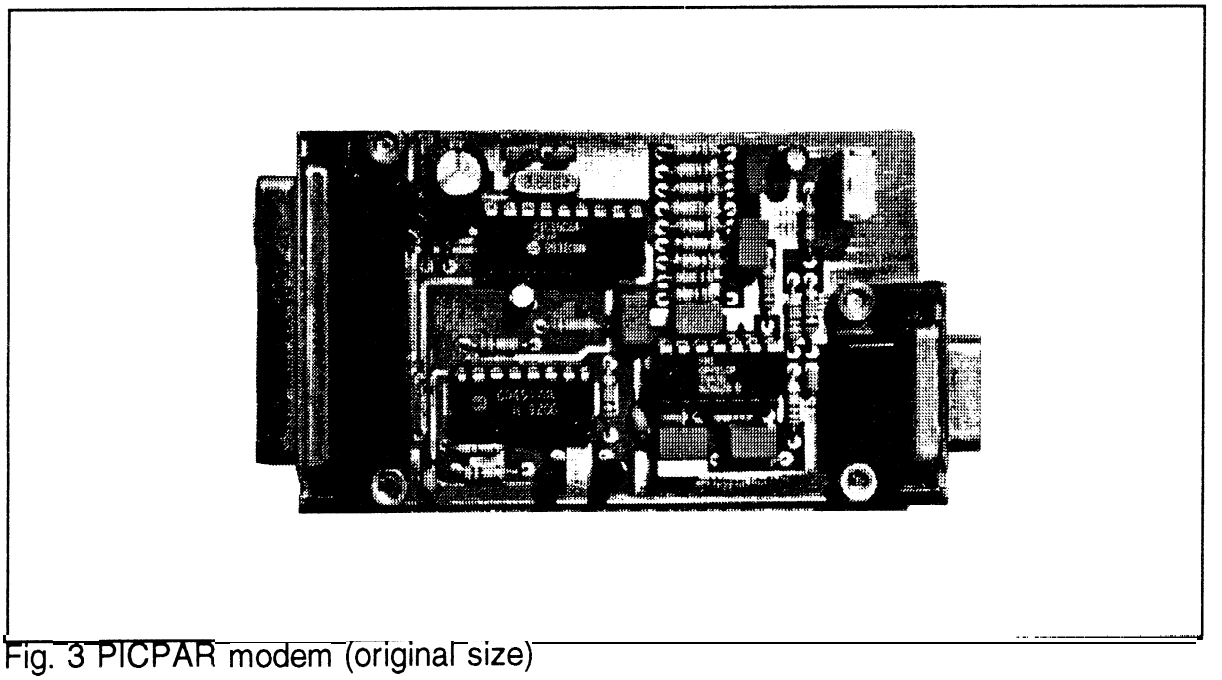

Fig. 3 PICPAR modem (original size)