FSK modem with scalable baud rate

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Introduction

Binary FSK modulation of the RF carrier is a well known and widely used transmission scheme for digital information. Old **RTTY** modems are the **first** example in amateur radio; nowadays packet radio is the most prominent FSK application.

The advantage of FSK is compatibility with existing FM voice radios and simple implementation, including robustness against misalignment, bad transmission characteristics of the radios, or **frequency** drift. More sophisticated RF modulation schemes are rarely used until now. Combined with coding techniques they could provide more efficient use of the RF bandwidth at low SNR but need very careful construction of both modem and transceiver. Subcarrier modulation techniques, like AFSK or AQPSK, are disadvantegous in respect to RF bandwidth and SNR.

Even succesfull digital cellular phone systems like the European GSM use GMSK (Gaussian minimum shift keying) which is basically FSK with controlled deviation and a baseband partial response **prefilter.** For this reason we believe that FSK will be used in packet radio for another long time.

Well-known amateur radio FSK modem concepts are those of **K9NG** and **G3RUH** which both use an additional scrambler with the polynomial $1+x^{12}+x^{17}$. Their implementations are different in detail but basically compatible at the air interface. **G3RUHs** filtering is more sophisticated with an EPROM hard-coded FIR filter in the transmitter to achieve best spectral purity without alignment.

Both are designed for 9.6 kbaud, need an RF bandwidth of about 20 **kHz** and work fine with IF filters down to **15 kHz.** They can be modified to other baud rates by changing a large number of parts in the analog filters and using another clock frequency. This can be useful to double the speed to 19.2 kbaud with slightly modified radios with 30 **kHz** IF bandwidth, or even more with broader **IFs,** like broadcast type **WBFM** circuits.

We have improved the **G3RUH** modem keeping in mind the idea of simple baud rate scalability through the clock frequency **[1,2].** This task can be solved by replacing the analog filters through switched-capacitor circuits combined with a completely digital DCD circuit. To care for birdies, broadband noise and other 'alias' effects of time discrete filter circuits some analog anti-aliasing filters are added which restrict the scalability to a range of **1:8** in baud rate, e.g. from **9k6** to **76k8.**

The use of **PLDs** in the circuit allow a compact design and a reduced part count. Additional functions like a bit regenerator for repeater-like 'data echo' operation at nodes are already included.

Hardware description

The modem circuit is shown in Fig. 1 (analog) and Fig. 2 (digital). These drawings are part of a larger circuit diagram of a complete node controller with the modem on-board so that the modem part numbering is not continuous, The circuit operates from 5V single supply. The operating current depends mainly on the type of the GALs used.

The interface to the node controller uses a baud rate x32 clock delivered by the SCC or equivalent which allows software control over the baud rate. The circuit assumes that the final RX clock is produced by the HDLC controller - if not it can be used from pin 19 of IC18 after inversion. The other lines are as usual (TxD, RxD, DCD, RTS, CTS). RxD and TxD must be NRZI coded. DTR has a special meaning (cf. next chapter).

IC13/14 form the TX scrambler; 8 outputs are connected to IC15 which contains the TX FIR lowpass filter. Its output data is DA converted by IC16 (output TFsk in Fig. 3). This part of the circuit is equivalent to G3RUHs transmitter but with less parts. It is important to note that the content of the EPROM IC15 is completely different from G3RUHs.

The analog TX filter is shown in the lower part of Fig. 1. The TFsk-Signal is fed to the input of IC27 which is a 8-pole Butterworth lowpass filter in switched-capacitor technique. Its comer frequency is 1/50 of the clock. We use the baud rate x32 clock to achieve a ratio of 0.64 between filter cut-off frequency and baud rate which is close to optimum.

The SC filter output is the filtered again through a 3-pole fixed frequency continuous lowpass realized by the additional opamp in IC27 and IC28B. It is dimensioned for the range 4k8-38k4, as shown, but the capacitors can be changed. The levels and gain of the stages has to be carefully chosen to avoid clipping at the low supply voltage.

Output connector, loopback jumper and other parts are not drawn in the diagram because they are application specific.

The receiver begins with a simple 2-pole fixed frequency continuous lowpass followed by another 8-pole SC filter. IC26 has Bessel characteristics resulting in minimal overshot. The high order results nevertheless in a good noise suppression. The output is threshold compared by IC28A; R15 introduces a weak hysteresis to improve stability.

IC18 (Fig. 2) samples the comparator output with the x32 “microclock”. It contains a DPLL and generates the RX clock plus a raw DCD information (DPLL locked/unlocked). IC22 and parts of IC21 form the descrambler while the other ICs serve for DCD processing.

JP4 allows the selection of a bit regenerating function to retransmit received signals on duplex user access points for monitoring purposes and collision avoidance. RxD is switched to TxD and PTT is activated when DCD comes up.

JP5-8 select the filter function as usual. 16 banks are available - 8 of them are filled with code in the moment.

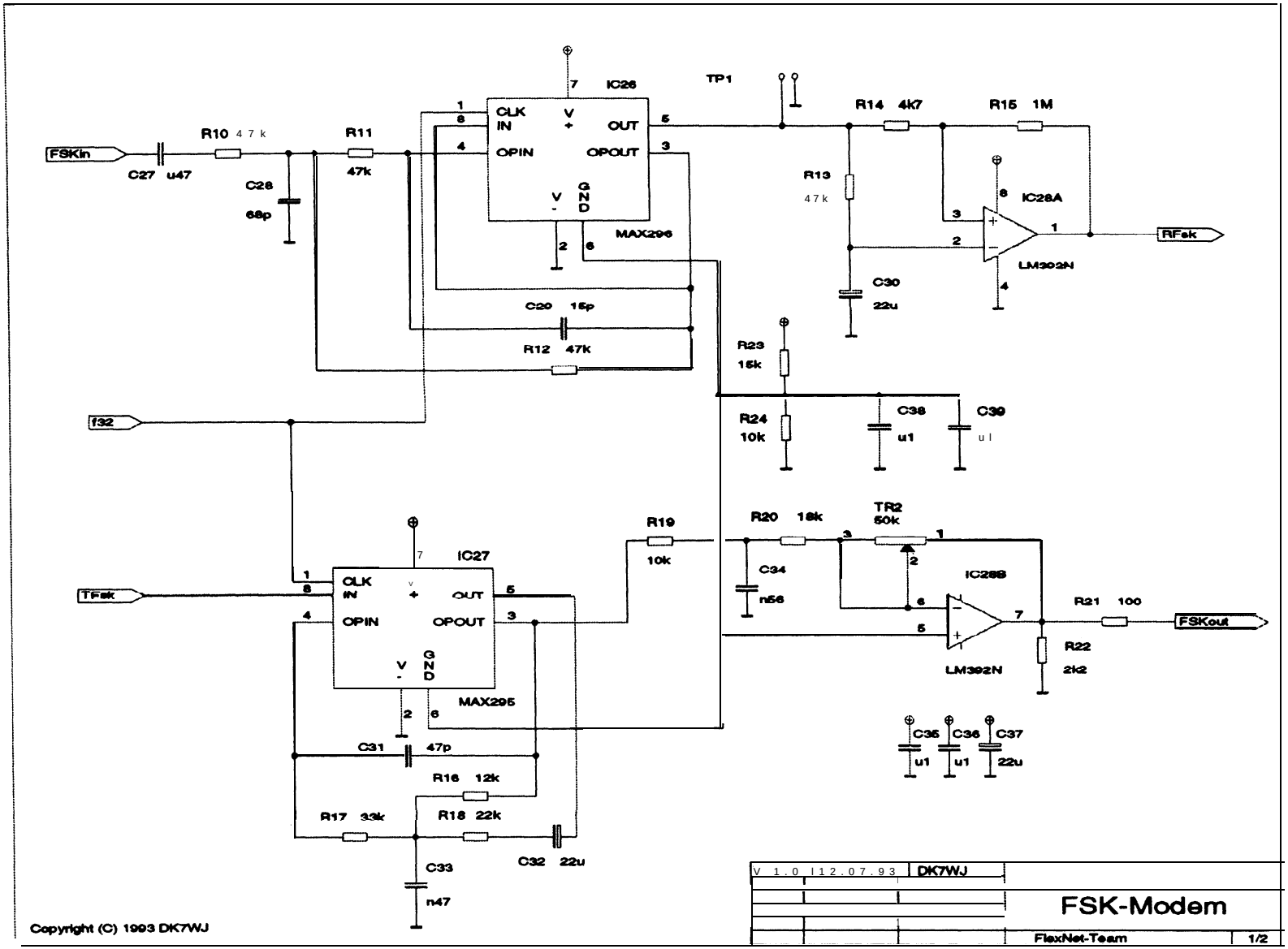

Fig. 1 Analog circuit

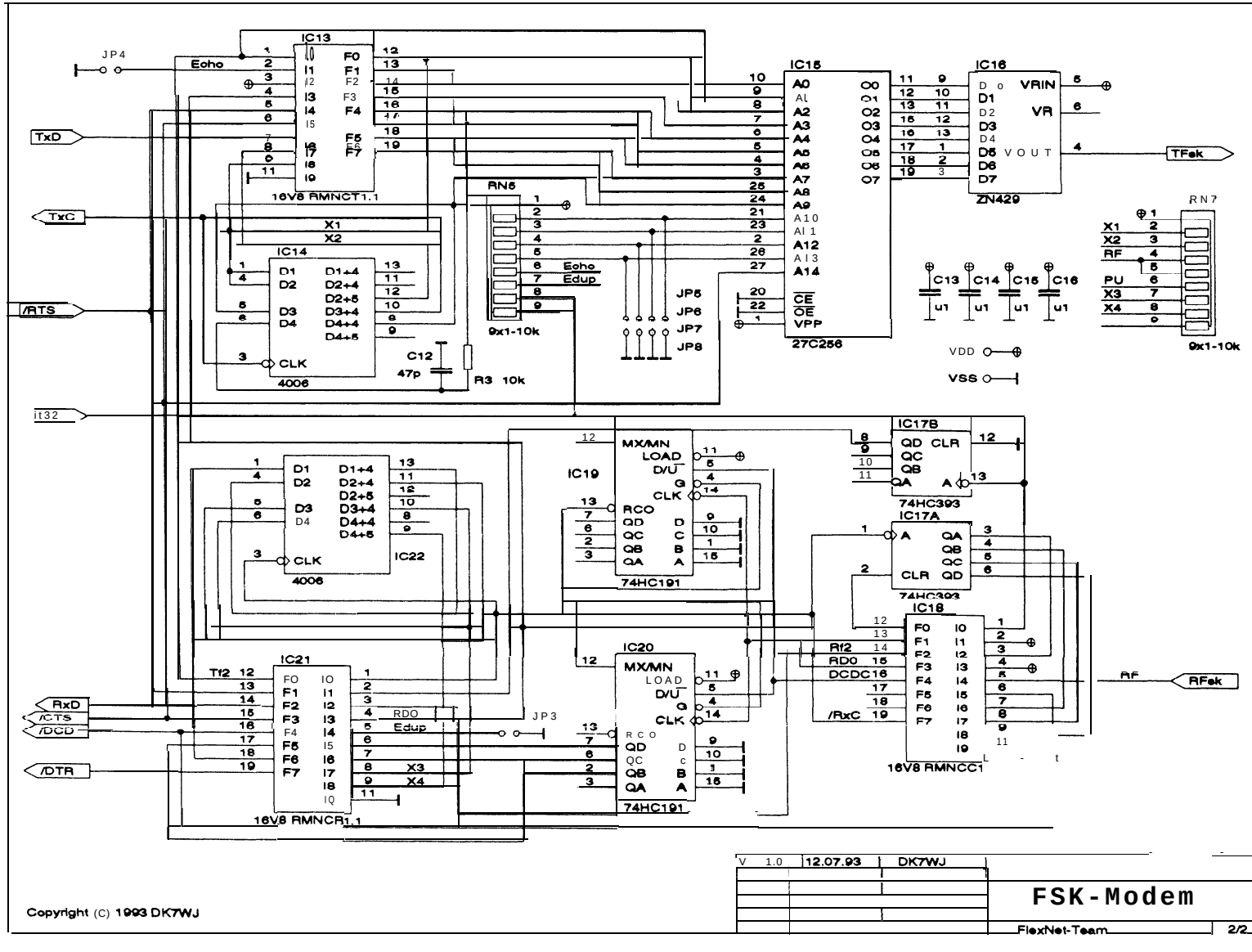

Fig. 2 Digital circuit

Filter design, DCD, and bit regenerator

There is a large number of filters of different types in the circuit. The transmitter signal is generated by the DAC with fourfold oversampling, e.g. during 9k6 operation 38,400 samples per second are generated from the EPROM table.

This results in a spectrum which can be tailored to the demands within a frequency range from DC to 19,200 Hz. Above there are unavoidable spurs called “alias” products.

To care for them the SC filter operating with a cutoff frequency of 6150 Hz has reached enough attenuation until 19,200 Hz through its high order. But this filter works in a discontinuous manner with a clock frequency of 307,2 kHz in our example. Clock f&through and up-converted signals around this frequency have to be removed again. The following 3-pole continuous filter with a corner frequency of 70 kHz provides enough attenuation at 300 kHz if the baud rate is 9k6, without introducing distortion to the signal in the case of 76k8 operation.

Fig. 3 shows the output spectrum of the modem operated with 9600 Baud.

The receiver circuit is equivalent but in the vice-versa order. The continuous input filter prevents the SC input from noise or IF signals at very high frequencies. The SC filter limits then the noise bandwidth to its final value.

The code in the EPROM is different from G3RUHs TX EPROM for the following reasons:

- one input line has inverse polarity which reflects in the data arrangement
- the target waveform has been derived independently [3] and might differ very slightly
- the analog postfilter is of a higher order and another type which is compensated for in the coded samples
- instead of the measured characteristics of some arbitrary radios the predistortion of the various waveforms compensates first order low pass filters of descending comer frequency
- the output voltage range is different

The code for both the GALs and the EPROM is free for non commercial use in amateur radio - ask one of the authors for files or samples.

The DCD circuit is a quite complex part of the modem. The soft 32-stage DPLL is the base for it. A signal is derived at each zero crossing which indicates if the crossing time was “good” (synchronous to the preceeding waveform) or ‘bad” (asynchronous). The discrimination threshold is dynamically ajusted to improve DCD speed and stability, between 25% of the frame interval1 around the transition of the DPLL when DCD is actually off, and 50% of it when DCD is on.

This DCD raw signal switches an &bit-counter to count up or down. It is clocked at 4 times the baud rate so that 6 bit are effectively in use. If more “good” than “bad” events occur it counts up and reaches a threshold where DCD is activated. This threshold has again a hysteresis so that deactivating occurs at a lower count. Both hysteresis are coded in the GAL circuit.

The complete DCD circuit is digital and synchronous to the x32 microclock so that it is baud rate transparent. No (fixed) integrating time constants are needed. The DCD response time is about 50 clock signals average (5ms at 9600 Baud) depending on tlhe signal quality. Even noisy signals produce no flicker.

The bit regenerator option is activated through JP3. On DCD response it switches the **PTT** line. If JP4 is also on it switches the source for **TxD** from the node controller interface to the own **RxD** line. The **TxC** is then derived the same way from the **RxC** out of the DPLL. So the received and retimed data is sent again.

If JP3 is on and JP4 is off only the **PTT** mechanism is active. Then flags (or whatever comes out of the HDLC circuit) are sent. In both modes the node controller has priority over the data or flag echo.

In addition this echo function can be enabled or disabled **from** the node controller through the DTR line. This allows remote control over the transmitter in case of interference (otherwise distant users would key the transmitter each time when the node receives their signal even if the node itself is off).

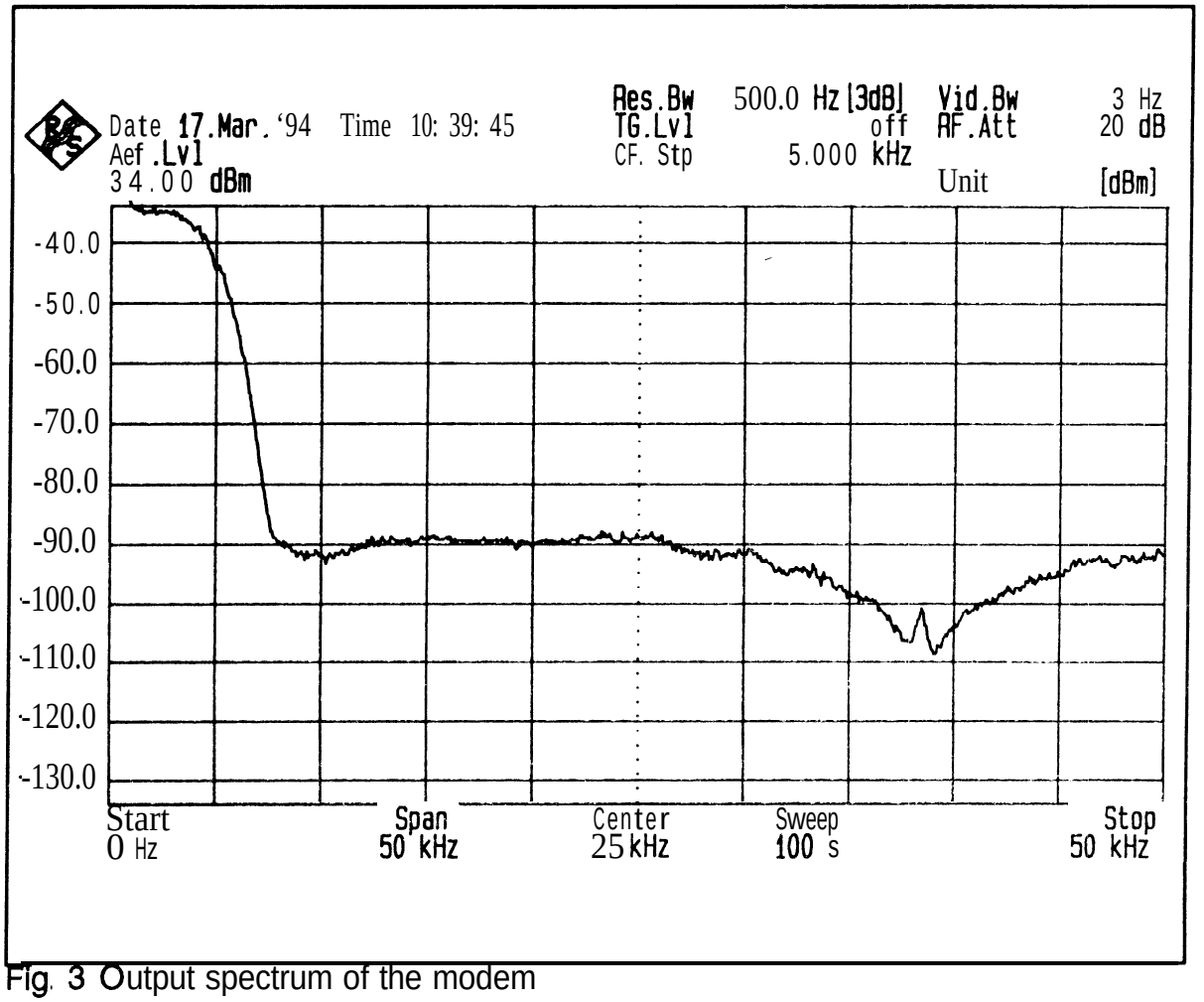

Fig. 3 Output spectrum of the modem

An implementation

We have implemented this modem on a European node controller board in 1993. The RMNC3 board contains the controller core with a HD63C09 processor, 64k RAM, 64k EPROM, an 85C30 for HDLC and a 65SC22 for a parallel bus to interconnect multiple controllers. In addition there was enough space for a TCM3105 for AFSK operation, a MAX232 for a KISS interface (e.g. BBS port) and the described scalable FSK modem.

It is a single port controller so that only one of the modems is used at the same time - with this configuration 99% of nowadays PR modulations can be realized with one board layout. Switching between the modems is not necessary because one proper board is used for each point-to-point link. Fig. 4 shows the asembled board (160x100mm, abt. 6.4x4 inches).

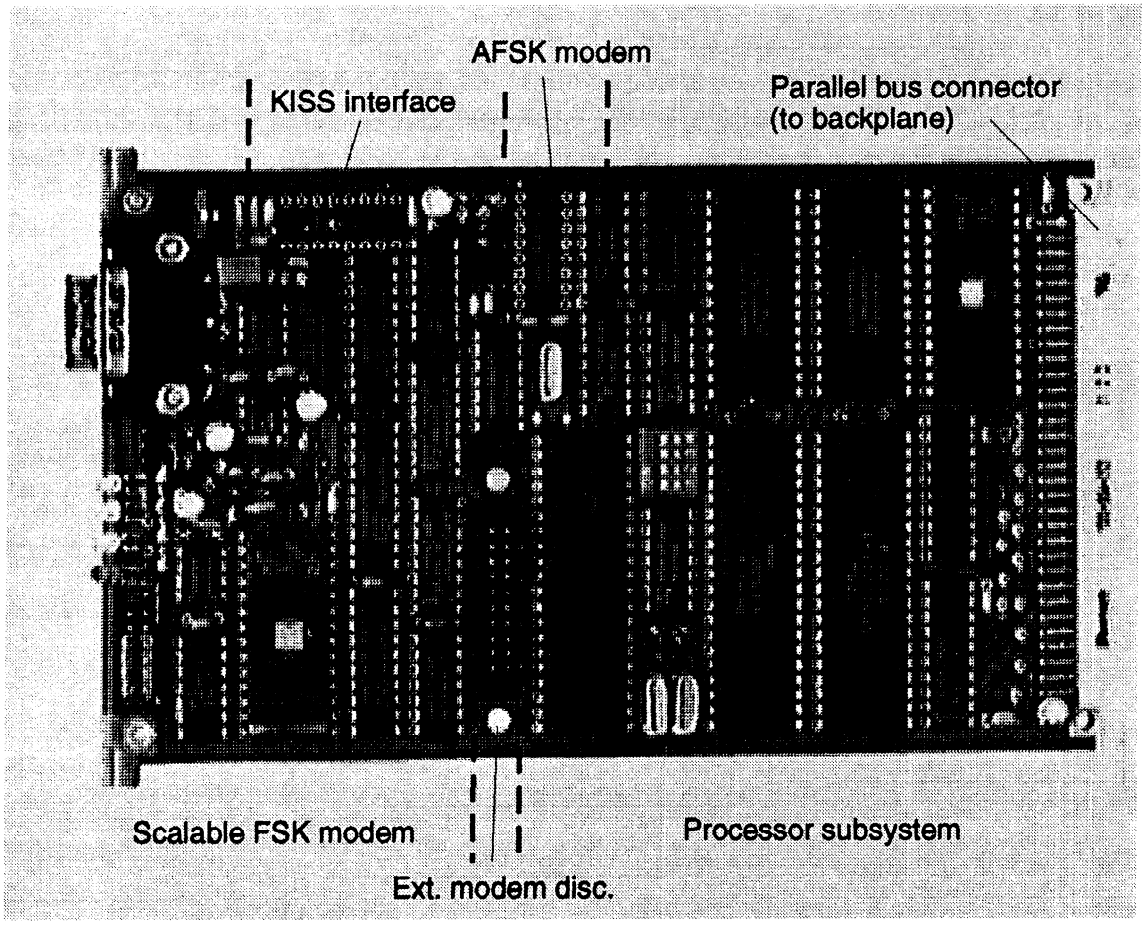

Fig. 4 Photo of an RMNC3 board with scalable FSK modem

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[3] Rech, W.-H., DF9IC: Iterierte duale Filterung - ein Verfahren zur Synthese von Datensignalen. ADACOM Magazin 6 (1993), 44-47.