HAPN-2: A Digital Multi-mode Controller for the IBM PC

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This paper describes a universal controller card for the IBM-PC bus. This system consists of one (or more) dual channel HAPN-2 adapter cards for packet radio. The basic card also has circuitry for experimenting with other modes such as RTTY, AMTOR, WEFAX, CW and SSTV.

Introduction

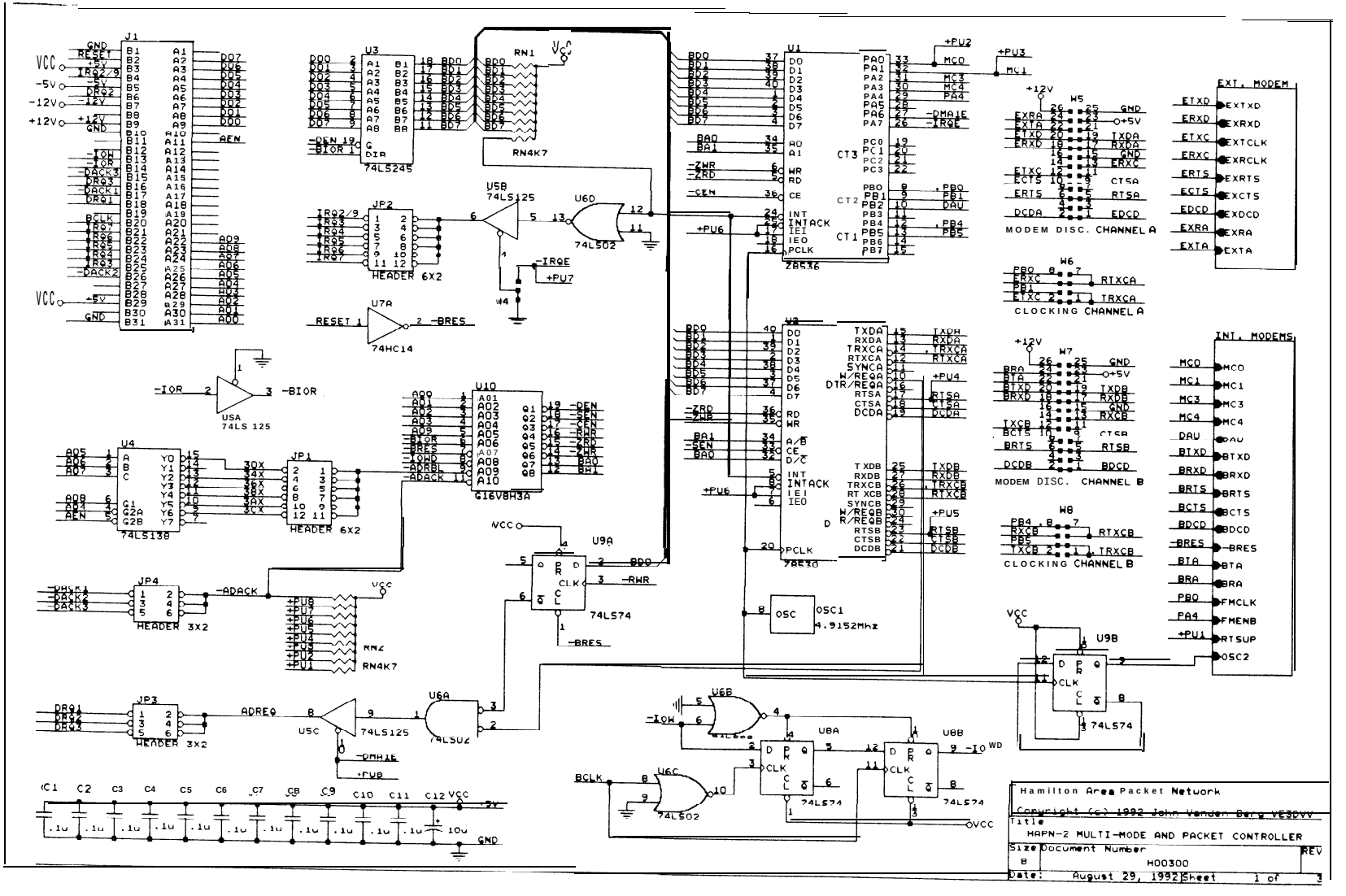
In 1985 we announced the first plug-in PACKET RADIO TNC for the IBM-PC (see Ham Radio Magazine, August 1986). The hardware and software were designed by the "Hamilton and Area Packet Network" (short HAPN) club, a group of experimenters. This card was called the HAPN-1 and was based on the now obsolete Intel 8273 SDLC chip. The card had one channel with a 1200 baud modem and used interrupts for operation. The card was also used with the HAPN 4800 baud medium speed modem (Ham Radio Magazine, August

the

driver

HAPN-2

8.6" x 4.24" (21.8 x 10.8 cm) as the HAPN-1 and has a small prototype area. It contains the ZILOG 28530 SCC serial communications controller and Z8536 CIO (counter timer and parallel I/O unit). The board supports 2 I/O channels for low and medium speed interrupt driven software. In addition Channel A can also be used under DMA control for real high speed modems such as the 56 Kb GRAPES modem. Channel B contains a AM7910 modern chip for conventional 1200 and 300 Bps (Bell-202 and Bell- 103) operation. Additional modems such as the 4800 and 9600 Bps can be accommodated by plugging in to one of the two modem disconnect headers piggy-back. The A Channel can also be connected to an external modem via a DB25 using TTL, RS232 or RS422 interfacing.


Hamilton Area Packet Network
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HAPN-2 MULTI-MODE AND PACKET CONTROLLER
Size B
Document Number H00300
REV
Date: August 29, 1992 Sheet 1 of 3
MODEM DISC. CHANNEL A
MODEM DISC. CHANNEL B
CLOCKING CHANNEL A
CLOCKING CHANNEL B
EXT. MODEM
INT. MODEMS
74LS245
74LS125
74LS138
74LS574
74LS502
74HC14
G16V8H3A
Z8536
Z8530
HEADER 6X2
HEADER 3X2
4.9152Mhz

The ISA PC-bus interface

For the PC interface refer to fig. 1, the main diagram. U2 is the dual channel Z8530 clocked at 4.9152 Mhz from an oscillator module. The maximum speed of operation depends on this clock as well as the operating mode. For synchronous NRZI encoded data such as is currently being used for packet radio, this works out to a theoretical data rate of' about 180 Kbit/sec. These speeds require fast DMA operation from the host computer. Higher speeds are possible by increasing the oscillator clock frequency and using external transmit/receive clocking. These high speeds rely on a short interrupt latency unless the CMOS version of the Z8530 is used. This chip contains more internal buffering for data and interrupts. A more practical expected speed for Radio packet is around 100 Kbit/sec on an ordinary 4.7 Mhz PC.

Chip U3 (74LS245) is a data buffer between the ISA bus and the adapter's internal data bus, and reduces the loading on the PC-bus to only one LS iload. The load of any one signal line on the PC-bus is **only** one gate. This loading is important when the user has all his slots in the PC filled up with cards. SIP resistors RN 1 provide the pull-ups for the internal data-bus. The adapter's address block is decoded with U4. The addresses of 30X, 34X, 36X, 38X. 3AX and 3CX are selections with JP1. The output goes to U 10 a PAL or GAL that does **the** remainder of the address decoding as well as controlling the DMA signal. U5B gates **the** interrupt request line to the **bus. The** card needs its own IRQ line and JP2 is plugged for the proper IRQ. Note that U5B can float the IRQ line if W4 is moved to enable the IRQE line. This can be handy if **the** IRQ is shared with a COM port (irq 3 or 4). The IRQ line would be floating after a reset and only be enabled when the software initializes the adapter **(activate** IRQE line). The diagram shows this feature disabled so the hardware would be compatible with existing DRSI PC-Packet drivers which do not support this feature. This same floating feature is used with the DMA lines DRQ1-3. Jumper JP3 selects the DMA request and JP4 the DMA acknowledge lines. Both jumpers have to be in the same position for the DMA to work. The DMA can also be quickly enabled/disabled by the DMA enable flip-flop U9A. This is done for short intervals during programming of the SCC. The dual D flip-flops U8A and U8B delay the leading edge of the IO write signal required for the NMOS version of the 28530. Both the 28530 and the 28536 CIO can generate interrupts to the system.

The Z8536 CIO

This chip contains **3** timers and a number of input/output lines. The I/O lines are used for enabling the DMA and IRQ signals enabling the adapter. PAO-3 are output lines and are used for the AM7910 modem. PA4 also going to the modem diagram (FMENB) selects between the AM7910 and the sine wave synthesizer to provide the transmit signal. The timers can be used in many different ways. When using the HAPNDRSI driver CT1 and

CT2 are used as divide by 32 for the transmit clock for the 28530 SCC. The CT3 timer is used to provide TX-delay and TAIL-delay for the packets. When running the DRSI NOS driver CT3 is used to generate 10 Msec interrupts for polling the SCC. Using the high speed HAPN-2 NOS driver CT1 is used for TX-delay and TAIL-delay for SCC DMA channel A with 1 msec resolution. CT2 is used in 10 Msec resolution for the slower channel. In other than packet modes such as WEFAX, RTTY, CW, etc. CT2 is used for generating the transmit signal and also for decoding of the receive signal.

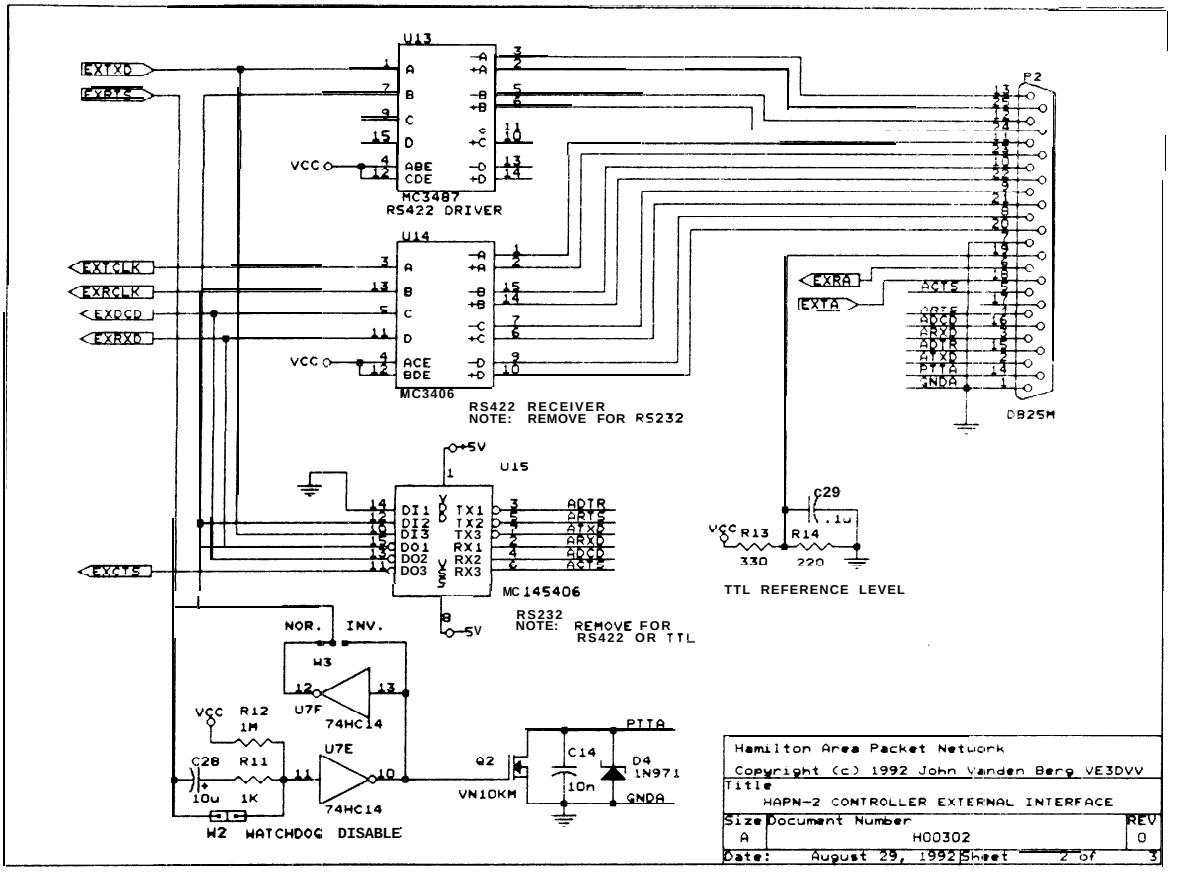
In short, the timers are handy to have around.

The Z8530 SCC

There are 2 versions of this chip, the basic NMOS version and the CMOS version. In this application we used the 6Mhz NMOS versions of the SCC and CIO chip. The CMOS version is really a better chip running faster, having more internal buffering and using less power, but is a bit more costly and not really required since the PCLK is only 4.9152 Mhz. The Cycle Recovering time, referring to the time period between any Read or Write cycles of the SCC is 6 PCLK cycles or about 1.2 microseconds. An input instruction on a basic 8086 takes 10 clock cycles, which on a 4.7Mhz XT (slowest PC I know of) works out to 2.1 microseconds. Considering other instructions usually used in a sequence, the SCC is certainly fast enough; however in fast 386 and 486 machines this Cycle Recovering time is important. Programmers have to put either a fixed or a variable delay in between successive I/O instructions. The variable delay would be determined by the programmer when actually measuring the speed of the computer.

The two channels on the SCC are independent of each other, and both have the same capacity when running in interrupt driven mode. The W/REQ line on channel A is brought out to allow this channel to work in DMA mode also. The HS modem is assumed to work half duplex in this mode. If more then one HS channel is required a second card can be added to the system. The A channel has no built-in modem, but supports an external modem either on the modem disconnect header W5 or via the DB25 connector on the back of the card. Selection of modem clocking between internal or external is done with jumpers on W6.

Channel B is the conventional slow speed packet channel for 1200 and 300 baud. However a medium speed modem could be substituted by installing the disconnect header W7. Control of clocking is done with W8.


U13
MC3487
RS422 DRIVER
U14
MC3406
RS422 RECEIVER
NOTE: REMOVE FOR RS232
P2
DB25M
U15
MC145406
RS232
NOTE: REMOVE FOR
RS422 OR TTL
TTL REFERENCE LEVEL
NOR. INV.
W3
U7F
74HC14
U7E
74HC14
W2 WATCHDOG DISABLE
Q2
VN10KM
D4
1N971
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HAPN-2 CONTROLLER EXTERNAL INTERFACE
H00302
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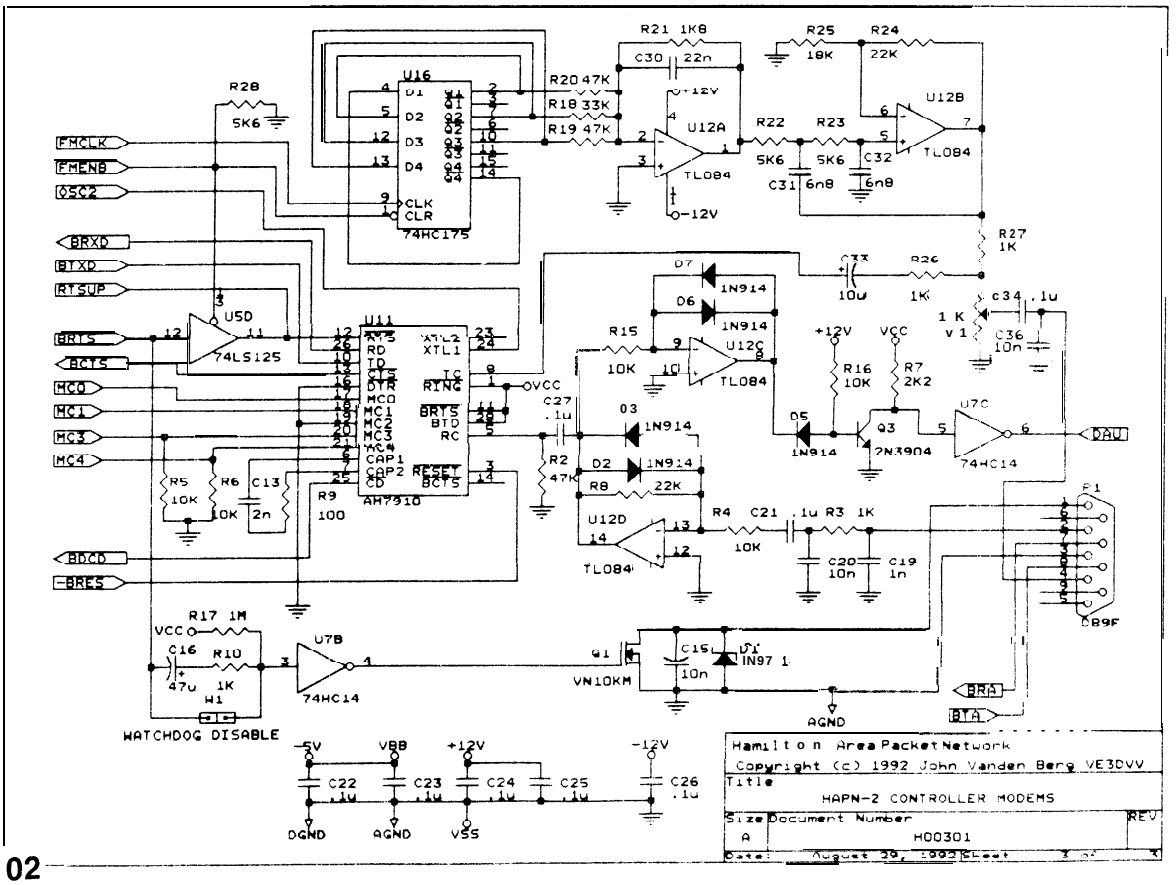
U16
74HC175
U5D
74LS125
U11
AM7910
U12A
U12B
U12C
U12D
TL084
U7B
74HC14
U7C
74HC14
WATCHDOG DISABLE
W1
Q1
VN10KM
D7
1N914
D6
1N914
D3
1N914
D2
1N914
D5
1N914
Q3
2N3904
P1
DB9F
DAV
BRA
BTA
AGND
DGND
VSS
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HAPN-2 CONTROLLER MODEMS
H00301

External modem interface for channel A

We have two options. The first is to use the modem disconnect header W5 with a. standard plug-in modem such as the 4800 and 9600 boards. The disconnect header includes the additional connections for power and audio in and out lines if one decides to use them (W5 pins 21 to 26). The second option is to use the DB25 connector for a modem outside the computer.

Refer to figure 2 for hook-ups via the DB25 connector on the card.
Schmidt trigger U7E with C28 and R12 produces a watchdog with a time delay of about 10 seconds. It can be bypassed with a jumper on W2 if required. Q2 is the driver for an open collector PTT line.

Selection between TTL, RS232 and RS422 is done by plugging in the appropriate chips. For RS232 levels only U15 (MC145406) is plugged in and U13 and U14 are removed.
The RS422 mode recommended for high speed is a TTL = like differential driver capable of driving long lines at high speed. Each signal requires 2 wires. A regular RS232 modem cable with all 25 wires can be used for hook-up. In this mode the RS232 chip U15 is removed.
For a TTL interface one could remove the interface chips altogether and plug in dip headers, bypassing the drivers. This is not recommended since the 28530 would not be protected from the interface and the drive capacity is very limited. A better way is to use only one half of the RS422 signals since the levels are TTL compatible. By using either the + or - inputs and outputs one can invert the signal between negative or positive logic true levels. R13/R14 provide a bias for TTL reference. In TTL mode the floating inputs of U 14 have to be connected (easily done in the DB25 connector) to this reference level at pin 3.9.

Built-in packet modem on channel B

Refer to fig. 3 for the built-in modems. U 11 is the AM7910 modem chip providing 1200 baud (BELL-202) and 300 baud (BELL-103). A third mode for 600 baud (CCITT V.23) could also be selected using the MCO, MC1, MC3 and MC4 control lines via the CIO. The clock for the modem chip is derived from the main oscillator module by dividing this frequency by two with U9b (main diagram). U12D provides soft input limiting with D2 and D3 for protection of the AM7910. The gain of the op-amp is set at about two with R8 and R4. Prefiltering of the input is done with C19, R3, C20 and C21. It is interesting to note that the AM7910 also has an equalizer circuit for 1200 baud that can be selected via the control signals.

Here is the AM7910 selection table:

MC4	MC3	MC2	MC1	MC0	
0	0	0	1	0	Bell 202 1200 Bps half duplex tones 2200 1200 Hz
0	0	0	1	1	Bell 202 1200 Bps + equalizer half duplex tones 2200 1200Hz
0	1	0	0	0	CCITV V.23 Mode 600 Bps half duplex tones 1700 1300Hz
1	0	0	0	0	Bell 103 300 Bps Orig loopback tones 1070 1270Hz
3.	0	0	0	1	Bell 103 300 Bps Ans loopback tones 2025 2225Hz

Note : For a complete list of modes refer to the AM7910 Technical manual available from Advanced Micro Devices.

Chip U7B (74LS14) is a hex Schmidt trigger used as a watchdog. The time constant R17/C16 make it kick in after about 30 seconds. By putting a jumper on W1 the watchdog can be bypassed. Q1 drives the PTT. The modems output is adjustable with V1 between 0 and .6Vpp.

Modem for other then. packet modes

Op-amp U12C will hard limit the receive signal and Q3 with D5 converts it to a TTL level by switching at the zero crossing. The schmidt trigger U7C shapes it to a fast rising pulse. The output goes to the trigger input of CT2 of the 28536. This circuit can be used for frequency measurement and demodulating CW, RTTY, AMTOR, SSTV, WEFAX etc. The sending part for these modes consists of the quad D flip-flop U 16 hooked up in a ring, driving three resistors of the digital to analog converter (R 18, R 19, R20 and op-amp U 12A) to generate a simple stair sine wave. The signal is filtered by U12B to produce a clean sine wave. The frequency of the sine wave is directly proportional to the clock frequency at pin 9 of U16. This signal (FMCLK) comes from the output of the Z8536 timer CT2. All that is required to produce an audio sine wave is to have the timer produce a square wave of 8 times the required audio frequency. The selection between packet and other modes is done by software, controlling the reset of the ring counter with FMENB and enabling the RTS for the AM7910 modem.

Conclusion

The design was made for the interest of the packeteer who looks forward for higher packet speeds and at the same time wants to enjoy the conventional 1200 Bps mode. Also it will let him experiment with other radio modes (CW, RTTY, WEFAX and SSTV) as well. These modes were added with little additional cost since most of the hardware was already present. TCP/IP networking at high and low speed are practical using NOS. The higher level software we had developed for the earlier HAPN-1 adapter can be used on the HAPN-2 as well due to the modular design and substitution of a different device driver. The board is available from HAPN in either assembled and tested form or in KIT form. For details contact H.A.P.N.

Note: The address of HAPN has changed!!

The new address is:

H.A.P.N.
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Mount Hope, Ontario
LOR 1W0 CANADA

Acknowledgements

I wish to thank Jack Botner (VE3LNY) for his software contributions and Max Pizzolato (VE3DNM) with the design of the circuit board.

References

[1] Heatherington, Dale, WA4DSY "A 56 kilobaud RF Modem" Proceedings of the 6th ARRL Computer Networking Conference Newington CT: ARRL 1987

[2] Botner, Jack, VE3LNY, Pizzolato, Max, VE3DNM, John Vanden Berg, VE3DVV "A PACKET RADIO TNC FOR THE IBM PC" HAM RADIO: August 1986