MICROSAT PROJECT - FLIGHT CPU HARDWARE

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ABSTRACT

AMSAT-NA is preparing a new class of satellite. Intended for low earth orbit (LEO), "MicroSat" will bring a new level of performance and flexibility to the satell i te user community.

MicroSat embodies bold advances in low-cost satellite engineering. A new approach to satellite flight computer design was required to attain mission objectives: low power, low cost, small volume and mass, high performance, high reliability. flexibility. significant mass data storage capability and high speed I/O.

This paper focuses on the design of the flight computer hardware and outlines some of its capabilities.

INTRODUCTION

The first planned launch of the MicroSat series is scheduled in early 1989 aboard an ESA Ariane-4 rocket. A total of four (4) MicroSats are scheduled to be aboard: two (2) uill be PACSAT missions [1], one (1) Will be a speech synthesizer for educational use (DOVE) and one (1) uill be a CCD camera experiment.

AMSAT, with support from TAPR, Weber State College (Utah), AMSAT-LU (Argentina) and BRAMSAT (Brazil), is designing and building these satellites on a fast-paced schedule. First proposed in late 1987. there will have been approximately one year elapsed time from concept to launch!

For the authors- it is reminiscent of the UoSAT/OSCAR-11 Digital Communications Experiment (DCE) schedule. The OSCAR 11 mission was proposed in late July. 1983. and de1 ivered to NASA for launch in January. 1984 (and launched March 1, 1984)! [2]

The PACSAT mission spacecraft will have five 2m uplink channels and one 70 cm down1 ink channel. The modulation techniques will be fully compatible with FUJI/ OSCAR-12 -- 1200 baud Manchester data fed to a standard 2m FM radio for the uplink and 1200 baud PSK data returned on the down1 ink. Eight (8) megabytes of message storage will be available on each PACSAT. Other data rates and modulation methods may also be experimented uith via in-flight hardware reconfiguration.

GENERAL DESCRIPTION

A typical MicroSat occupies a cube about 9 inches on a side. The CPU module occupies a slice about 1-1/2 inches thick. The CPU power budget is only 1.5 watts.

The CPU module occupies two (2) PC boards and provides the following resources to the satellite:

- Six (6) serial I/O ports capable of multiple protocols.
- Six (6) channels of manchester decoding in the receive signal paths (five standard user and one special purpose).
- One (1) serial I/O port dedicated to telemetry gathering and control of the various spacecraft modules. experiments and systems.
- Six (6) DMA channels.
- 256k bytes of error detecting and correcting (EDAC) memory.
- Two (2) megabytes of RAM organized as four (4) 512k byte banks with dual-port access. .
- Eight (8) megabytes of RAM organized as a serial-access pseudo-disk.
- One eight-bit A/D for analog signal measurement.
- Reference voltage for telemetry systems throughout the spacecraft.
- Eight (8) I/O ports mapped for external experiment support.
- Watchdog timer to automatically reset the CPU upon detection of a CPU crash.
- Ground control reset capability in case all else fails.

SPECIAL FEATURES

The CPU module utilizes CMOS logic and CMOS LSI chips throughout. It employ8 a true multitasking kernel and takes advantage of a reduced power wait state when the task scheduler al lows. To reduce volume requirmeents, surface mount technology (SMT) ICs are used where available.

The microprocessor selected is the NEC 70208 (V40) CMOS integrated device. This IC contains a superaet of the Intel 8088 microprocessor (including added instructions and reduced cycle times for a given clock speed) along with several peripheral functions The on-chip peripherals include: clock generator: four (4) channel DMA controller (71071-compatible); UART (8251-compatible subset); three (3) sixteen-bit programmable timer/counters (8254-compatible); eight (8) input priority interrupt controller (8259-compatible); programmable wait-state generator and bus interface logic/drivers.

Additional DMA support is provided by a NEC 71071. a high-performance CMOS four (4) channel DMA controller. In conj unction with the V40 CPU. and allowing for the various modes and features used in the system. a total of six (6) ueab 1 e DMA channels result.

Serial I/O (72001) chips are also from NEC. These devices are similar to the Zi log Z85C30 SCCs used in some Amateur packet applications, but provide a number of interesting benefits. The most important ones are (a) ability to interface to the V40 and 71071 with a reasonable amount of discrete logic glue and (b) independent programmable baud rate generators for each transmit and receive channel.

A Harris 2k byte CMOS fusible-link PROM is used for bootetrap memory. A smaller version of this same device was successfully employed for the same purpose in the UoSAT DCE.

EDAC

The EDAC memory posed an interesting challenge. This type of memory is necessary to store program code. vectors and certain data that cannot be al lowed to become corrupted due to radiation effects.

The UoSAT DCE has 16k bytes of EDAC protec ted memory. The authore proposed a whopping 64k bytes of EDAC for MicroSat based on the availability of 64k by 1 CMOS memory chips. Surely. this should be enough memory for such a small satellite!

However. the software coders had other ideas and made it abundantly clear that at least 128k bytes of EDAC memory was needed and even more would be desirable.

The problem. a8 with most things in this roject, is that there just isn't much PC board area to cram ICs onto. and insufficient volume to easily stack more than three PC boards into. The EDAC memory utilizes twelve (12) memory chips to save enough information to recover from a one-bit error in each eight-bit byte.

Fortunately. 256k by 1 CMOS static RAMs became available in very limited quantities by June of 1988. The specifications for the chips were discouraging - they would apparently require a tremendous amount of power while operational. The price was only slightly more intimidating. Measurements. however. indicated power consumption would be manageable in this application. Successful operation of the wire wrap prototype running a program from the EDAC memory in early August of 1988 confirmed the earlier power consumption measurements.

Twe 1 ve Hitachi 6207 256k x 1 ICs are employed as the storage elements in the EDAC memory array. with a combination of 74AC and 74HC logic to provide buffering. syndrome encoding and decoding. and detected error logging. This memory occupies the lowest 1/4 megabyte of the V40 address space.

OTHER MEMORY

OSCAR 11's DCE demonstrated that conventional static CMOS bytewide RAMs would perform satisfactorily in low earth orbit [3]. Such memory requires software protection schemes to detect and errors in stored data. They are unsuited for program storage.

In the MicroSat CPU address space. the middle 1/2 megabyte is filled with such memory. A total of two (2) megabytes are located on the CPU main PC board. organized as four (4) banks of 1/2 megabyte each. Each bank is under control of the CPU and can be independently powered on or off. se1 ec ted for access by the CPU or selected for access by an external experiment. This "dua1 porting" arrangement allows external devices (such as the Weber State CCD camera) to have high-speed access to memory for storage or retrieval of data as well as communication with the CPU. It also protects the CPU buses from any sort of malfunction by the external device.

Since the CPU controls the spacecraft as well as manages the experiments. CPU health is paramount to mission success. Hence, the dual port arrangement rather than allowing experiment access directly to the CPU's buses.

MASS STORAGE

It was determined that a total of two (2) megabytes of non-EDAC RAM is insufficient to support a PACSAT mission. especially when second-generation missions are flown with higher data rate radio channels. Speeds of 56 kilobits per second are envisioned in the near future for PACSATs, and higher data rates soon thereafter. For this reason. additional memory is required.

On the other hand. many MicroSat mission8 may not require large amounts of memory. in which case the bank-switched two (2) megabytes will suffice. At a review meeting in Boulder. Colorado, in June of

1988, WA4ONG suggested a serial-acce88 mechanism be employed to allow a low-power, high capacity data atorage device to be built on a separate PC board. This idea was adopted.

The mass storage board contains programmable address counters that may be written and read by the CPU. A 24-bit address bus is employed on the unit, allowing up to sixteen (16) megabytes of storage. Present chip8 limit this to 8 megabytes, but by mid-1989 it should be possible to build a 28-bit address bus unit (256 megabytes!) with at least 32 megabyte8 populated on the same size card!

The entire mass storage unit occupies eight (8) bytes of 110 space in the V40 address map. The address counter is auto-incremented following every memory read or write, so block move instructions may be employed to rapidly move chunk8 of data between mass storage and directly addressable CPU memory.

DMA

In order to provide capacity for high-speed data 1inks, DMA techniques are employed in the CPU between the V40 and the 72001 serial I/O devices. Under DMA, the CPU ha8 only to set up the DMA controller and serial I/O chip, then go on to other tasks. After the data is sent or received, the CPU will be interrupted. This greatly reduce8 the processing power needed to manage communications and allow8 for very rapid data link rate8 on multiple channels.

GENERAL LOGIC

Final ly, it should be noted that programmable logic devices are not utilized in the CPU design. Currently available CMOS devices are either EPROM or EEPROM based (and thus susceptible to radiation damage) or too slow (Harris fusible link PALs). RAM based device8 (Xilinx) are under investigation for future generations of MicroSats, but appear inappropriate for the present. Bipolar devices consume far too much power.

In 0rder to achieve the required speeds with unknown capacitive 1oads, AC 1ogic is generally employed. HC logic was used in the OSCAR-11 DCE and has performed well. AC logic will get its shakedown with the first MicroSats. The designers of the CPU think that the ground bounce spike8 made famous by the designers of alternative pinout logic will not be a problem since such transients have plenty of time to subside at the relatively slow bus speed of the MicroSat CPU.

CONCLUSION

MicroSat provides a low cost spacecraft bus upon which various experiments may be flown. PACSATs will occupy tuo of the first four MicroSats. The MicroSat CPU is flexible and powerful, allowing significant growth in future mission capability without redesign.

It is the authors' hope that, uith the successful launch of the first cluster of MicroSats, Amateur packet radio networking will take another giant step forward.

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