THE AMSAT/TAPR DSP 1 PROJECT: HARDWARE DESIGN

by

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BACKGROUND

A couple of years ago, Tom Clark, W3IWI and Bob McGwier, N4HY, began involving a number of Amateurs in applying digital signal processing (DSP) techniques to Amateur radio.

Recently, AMSAT and TAPR have combined forces to jointly develop and distribute DSP hardware and aoftuare for the Amateur community. Tom and Bob have written fairly extensively about the potential appl icationa of DSP in the Amateur environment.

The first hardware fruits of this marriage is called DSP 1. This paper is intended to provide a deeign overview of the DSP 1 harduare conf iguration.

HARDWARE OVERVIEW

The DSP 1 is designed as a eet of PC boards that can be configured to indivi- dua 1 requirements. A t a minimum, the system consists of a metal cabinet' an I/O board, a DSP board, a power supply board and a loader board. In place of the loaders a general purpose processor (GPP) board can be inatalled for greatly en- hanced operation and flexibility. For all but the simplest applications the GPP will be required.

This breakdown of function to PC boards has the advantage of allowing upgrades at reasonable cost, providing flexibility for adoption of future standards or refine- ments in interfaces, and simpler trouble- shooting. It has the disadvantage of increasing initial costs Somewhat.

Cabinet

The system is designed around a Ten Tec B- series enclosure. This is an all metal, low profile box that can be shielded for RFI/EMI. The use of this enclosure in- creases costs over the type of case used by a TNC 2, but is less expensive than the "Gucci" cabinet used with the TNC 1.

I/O Board

The l/O board mounts on the back panel of the cabinet. All connections to the out- side world are handled through this board. This allows internal interfaces to run at TTL levels for digital signals and -5V to +5V levels for analog signals. It also simplifiea construction for the kit builder, eliminating uiring harnesses.

BY standardizing al 1 interface signal levels. future DSP and GPP boards may be deve 1 oped to utilize improved technology without rendering DSP 1 obsolete. Future standards in radio and serial I/O inter- face levels can also be accommodated by replacing the I/O board rather than a far more expensive DSP or GPP board.

All connectors are well lbypassed to ground for EMI/RFI. Radio interfacing (PTT, CW keying, microphone audio, speaker audio. up/down control , etc.) is hand 1 ed here. along with level translation and filter- ing. Two radio ports are provided.

Serial I/O ie handled at RS232 levels. Again, all level translation is handled on the I/O board.

A special TTL-level connector compatible with the modem disconnect arrangement used in TAPR TNCs and the TAPR PSK modem is also provided for those users who wish to use the DSP 1 as an external modem for an existing TAPR-compatible TNC.

Final ly, power is routed into the DSP 1 through the I/O board for consistent fil- tering.

DSP Board

The initial DSP board is based on the Texas Instruments TMS320C15 processor. This is a first-generation DSP chip with some enhancements over the earl ier TMS320 10. It is run at a clock speed of 25 MHz, and has a full 4k words of high- speed static RAM for program memory.

An AD7569 eight-bit analog I/O port made by Analog Devices is: used, and the board has provision for two such ports. Eight bits provide for over 40 dB of dynamic range, more than most radios provide at their audio outputs. More bits are useful for test equipment, but significantly increase the cost of the device.

Anti-alias filtering is generally required for any analog to digital converter. This filtering is provided in the case of the DSP 1 by a Gould S35.28 programmable low

pass filter. This filter provides a 7th order elliptic function with with stopband attenuation beyond the dynamic range of the 8-bit A/D converter. Placing it8 frequency cutoff under direct control of the DSP chip provides maximum flexibility for applications programmers.

A multiple channel programmable timer (82C54) is mapped in the TMS320C15 I/O space and may be used to generate interrupts and/or control the sample rate of the A/D and D/A. A phase shifter. designed by WB6HHV, allows the DSP chip to lock onto the external signal, allowing reduced sampling rates for a given signal after acquisition. This is a feature not normally found on DSP analog front ends. and should prove very useful in many applications.

Digital I/O is handled through CMOS eight-bit latches. This allows the DSP board to connect to a TNC and exchange TTL level data with the HDLC chip, thus acting as an external modem.

The 4k word memory has two access paths. An external device (loader or GPP) can suspend the DSP chip, access the 4k word area as an 8k byte area, and read or write to it. This is how the 32015 programs are loaded.

There is a series of single-bit latches provided to synchronize information exchange between the DSP and GPP boards for high-speed data transfers. Eight-bit latches are used to store the information bytes transferred in this manner.

Address mapping and general purpose logic functions are bundled into a reprogrammable logic device (Lattice GAL (r) or equivalent) to allow reconfiguration and reduction of parts count on this board.

CMOS parts are used exclusively for minimum power diesipation.

(A Look Ahead)

The next generation board (DSP 2) will have considerably more processing horsepower (Motorola DSP56001 or TMS320C25), memory and analog I/O resolution (12, 14 or 16 bits). It will probably contain FIFO buffers for all I/O. It will be designed to retrofit into the DSP 1 cabinet and utilize the GPP and other resources.

Power Supply Board

The power supply board provides regulated +5, -5, +10 to +12 and -10 to -12 volt8 from an unregulated +12 VDC nominal source. It utilizes switching techniques for efficiency, although the initial board may use simple charge pumps. There is nothing particularly unusual about this board.

Loader Board

The loader board is intended for low cost, modem-only applications. It allow8 the user to select from a number of programs stored in a single EPROM (4 programs in a 27C256, 8 in a 27C512). A press of a button halts the DSP board, loads the selected program into the DSP memory, then restarts the DSP engine. This board uses only a few standard CMOS logic functions and will be very inexpensive (excluding memory!).

GPP Board

The GPP board allows the DSP 1 system to become a highly flexible and very powerful communications tool for the Amateur.

The GPP is based on the NEC V40 integrated processor and 72001 serial I/O chip. This allows software to be developed and debugged on a standard IBM PC (r) or compatible system, This board features two serial channels running full duplex under DMA, allowing high speeds to be attained for use with such devices as the Heatherington 56 kbps modem.

Four (4) 32-pin bytewide sockets allow up to 1/2 megabyte of memory, with 64k bytes a typical minimum configuration. Battery-backed RAM and a CPU watchdog are included, along with a Centronics compatible parallel printer port.

CMOS logic and CMOS LSI are used exclusively in the GPP for reduced power consumption and high reliability. Programmable logic devices contribute to hardware design simplification.

Bytewide I/O ports to and from the GPP board allow high-speed data transfer with the DSP card. In addition, serial I/O supporting multiple protocols can be used to exchange data with the DSP section.

The net result is a truly flexible and powerful communications device. Narrow-shift RTTY (30 Hz shift for 60 WPM, for example), tracking filters, efficient HF packet, SSTV and FAX applications all become possible without compromised modem performance.

WHITHER SOFTWARE

The Dalanco-Spry Model 10 is being used by a number of Amateurs in the context of the overall DSP development project. This unit is a plug-in card for IBM PCs and compatibles. It allows development and testing of software for the TI 3201x processors. As such, it is an excellent development tool for the DSP 1.

There are a number of applications that have already been written and used by several Amateurs, including moonbounce work with OSCAR-class stations, weather

sate1 1 i te image decoders with software modems. PSK modulators and demodulators, etc.

In the case of DSP 1, the software is waiting on the hardware!

VRAP UP

The DSP 1 project represents a major effort by AMSAT and TAPR to provide the Amateur community with advanced* affordable technology to enhance digital communications. It provides a modular, flexible platform for experimentation and continuing development, in this field.

A8 the technology represented by DSP 1 becomes commonplace in the ham shack, the need for new hardware to use new communications modes should become significantly reduced. For example, in order to use FUJI/OSCAR 12 or one of the new MicroSat-based PACSATs, one presently needs a PSK modem accessory for his TNC. Such a modem costs about $100 as a kit or $200 assembled. A DSP 1 arhould sell for less than the TNC and PSK modem combination. yet provide as much flexibility for the Same specific application. It will also do numerous other things well, such as a multimode digital controller (like the AEA PK-232 or Kantronics KAM or MFJ-1278), or a special-purpose communication8 device (multi-level SSTV or WEFAX or weather satellite FAX decoder).

Digital signal processing techniques promise improved reliability in communications. The DSP 1 will help bring these techniques to Amateur radio.