A Networking Nods Controller for Amateur Packet Radio

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Introduction

Perceiving the need for a standardized hardware environment for developing, testing and implementing Amateur packet radio network and transport level protocols, the author, under the auspices of Tucson Amateur Packet Radio (TAPR), conducted a three month discussion with leading packeteers in the United States during the summer of 1985. The intent was to define the hardware desired in a controller that would be suited to this task. Having reached a general consensus, a system was designed which incorporated most of the suggestions of the group.

The resulting system, the TAPR Network Node Controller (NNC), is currently in its third hardware revision. It is expected to be placed in the field during the second quarter of 1986 for software development and system testing. It is hoped to be available to the general Amateur packet radio community during third quarter 1986.

This paper describes the features of the NNC that make it a logical choice upon which to build an Amateur packet switching system.

Networking Background

The most prevalent protocol in Amateur packet use today, AX.25 Level 2 Version 2, is a link-layer protocol providing single--point to single--point connectivity. In an effort to expand a typical VHF station's RF domain, an expanded address field which allows for digital repeaters (digipeaters) is included in the protocol definition.

Digipeaters are a mixed bag. They have allowed stations to communicate beyond their normal radio horizon, as intended. This feature has been a positive contributor to packet growth. In addition, so-called wide area digipeaters have aided in placing packet-dedicated RF facilities in useful locations for future networking. At the same time, digipeaters have contributed to present-day channel congestion due to the end-to-end acknowledgment used as opposed to using point-to-point acknowledgments along the digipeating path.

Network-level protocols (used loosely in this paper to include appropriate features of transport-level protocols as well), on the other hand, generally provide for hop-by-hop acknowledgment. This helps reduce channel loading, improving channel efficiency and throughput. There are many other features that networking will eventually provide that are beyond the scope of this paper.

NNC Hardware Requirements

A networking controller should be capable of handling multiple simultaneous RF channels to allow it to switch and otherwise (re)route traffic. In addition, it may need relatively large amounts of memory storage to handle buffering of multiple packets. It should also be rugged in order to reliably serve in harsh, remote sites (mountaintops, for example).

An Amateur NNC, in addition to the above requirements, should also be very inexpensive, expandable and use a processor for which there are many familiar and available software tools.

NNC Digital Hardware Description

The TAPR NNC design meets these objectives.

A total of four HDLC ports are included on the digital board. With appropriate modems and radios, this allows up to four radio channels to be used simultaneously. The ports are implemented in hardware for speed, are capable of using full-duplex packet channels and are configured for vectored interrupt operation. In addition, two of the four ports may be operated under direct memory access (DMA) control for very fast channels. These ports are based on the Zilog (tm) SIO/2 chip, a dual-channel device proven in Amateur packet use (eg, the TAPR TNC 2 uses an SIO chip for HDLC operation>.

The microprocessor (uP) chosen for the NNC is the Hitachi HD64180. This CMOS engine incorporates a number of functions usually associated with external peripheral ICs. In addition to the uP core, which is a superset of the familiar Z-80 (tm), a pair of asynchronous serial input/output (I/O) channels, a dual-channel DMA controller, a priority interrupt controller, a programmable 16-bit timer counter, a clock oscillator and a primitive memory management unit (MMU) are all included on this single-chip device.

The MMU allows a total physical address space of 512 kbytes to be utilized by the UP. A paging scheme is employed to divide the physical address space into three logical address spaces. The net result is a fast and relatively efficient expansion of the normal 64 kbyte address space limitation of the Z80.

Memory on the NNC is physically organized into two banks of eight bytewide sockets each,

The lower bank, mapped into the first 256 kbytes of physical address space, includes a hardware wait-state generator that is activated on op code fetches only, allowing the use of inexpensive 250 nSec EPROMs to contain program code. Each of the eight sockets is individually configurable, by means of on-board Jumpers, to utilize a 32 kbyte EPROM or an 8 or 32 kbyte static RAM IC. Each socket consumes 32 kbytes of physical address space, regardless of the XC installed at a particular location.

The second bank of sockets is intended for low-power CMOS static RAM only. This bank is battery-backed, allowing up to 1/4 megabyte of non-volatile RAM to be included on the NNC. A single Jumper on the board configures these eight sockets for 8 kbyte or 32 kbyte RAMs. These parts cannot be intermixed in this physical bank of memory. No wait-states are inserted during op-code fetches in this area of memory, since 150 nSec (and faster) RAM is readily available at low cost.

The IC used to control the battery-backed RAM (bbRAM) circuitry allows testing the condition of the battery every time the NNC is powered up from a battery-backed state. Software routines may utilize this feature to report impending battery failure.

For future expandability, an industry-standard Small Computer Systems Interface (SCSI) port is included on the NNC. The SCSI port may be DMA controlled, or simply interrupt driven. This port should be capable of transferring data at rates up to 1.5 megabytes per second, allowing the NNC to act as a "front end" processor for later high-capacity data concentrators as the Amateur packet network evolves-

A pair of eight-bit parallel ports are included in the NNC. One is configured as a Centronics (tm) compatible parallel printer port, the other as a general purpose I/O port. These software controlled ports may be used for modem reconfiguration, direct control of an rf deck, controlling status indicators or other purposes.

The HDLC and parallel ports utilize an interrupt method known as Mode 2 on the UP. This allows the interrupting peripheral IC to identify itself to the uP at the time the interrupt is acknowledged, resulting in a very efficient interrupt structure. Further, software ompatibility with the 280 opens the door for many experimentally inclined packeteers to develop, test and refine the software used on the NNC.

In order to encourage such experimentation, a second PC board was developed for the NNC. This board simply plugs onto the NNC digital board and provides a complete, DMA-capable floppy disk controller. Up to four floppy disk drives may be operated by this controller. ZRDOS (tm) or CP/M-80 (tm) operating systems may then be run on the NNC, assuming a proper BIOS and bootstrap ROM are available.

The floppy disk adapter is based on the Standard Microsystems FDC9266 controller, which is an integration of the NEC uPD765 controller with data separator circuitry.

Modems

A third PC board contains a set of four modems as well as a tuning indicator.

The modems are based on the XR2206 and XR2211 FSK modem ICs. These are low-speed (1200 baud default for three, 300 baud for one) modems intended to provide access to the NNC by Amateur stations using standard TNCs. The 300 baud modem is connected to the tuning indicator for ease of use on HF.

Unlike earlier TAPR modems these contain no switched-capacitor input filtering. A passive filtering system is used, resulting in simplified circuitry. The demodulators have been tested in the prototype modem board and a signal of 5 mV peak to peak has been shown to be sufficient for stable capture and lock of the PLL. This high sensitivity is due in part to the use of the XR2211 demodulator IC, in part to the use of a four--layer PC board and in part due to careful selection of modem operating parameters.

The modem board includes a crystal-controlled baud rate generator and each modem includes a state machine to recover clock information from the incoming NRZI data stream. In addition, circuitry is included to convert the NRZ data from the SIOs on the digital board to NRZI for transmitting purposes. A watchdog timer is included in each modem to guard against inadvertent lockup of a packet channel.

The modem board is extensively decoupled to prevent RFI. Similarly, it is designed to be resistant to conducted (incoming) EMI.

General

All boards in the NNC are four layered. This provides an extensive ground plane and power plane for each board, reducing

noise and easing decoupling of the various ICs.

The digital and modem boards conform to the physical form factor outlined by the California WestNet group. These boards are 5.75 by 7.75 inches and include mounting holes to allow them to be attached to the bottom of a standard 5-1/4" floppy disk drive. The power connector is identical to those on such drives, as is the pinout of the power connector.

The floppy adapter card, which piggybacks onto the NNC digital board, has mounting holes which align with those of the digital board when the cards are interconnected. It obtains power directly from the digital board,

The NNC is designed around CMOS circuitry wherever possible. Applying this technology results in wider noise margins, less heat and lower power consumption than other approaches. The net result is increased reliabilty.

Summary and Conclusion

The TAPR NNC is the result of design suggestions from experienced packeteers all over the U.S. It incorporates features making it easy to develop software for, implements a philosophy leading to high reliability and provides a common hardware base tailored specifcally for networking protocols in the Amateur packet environment.

At the beginning of 1985, there were perhaps 2,500 Amateur packet radio stations. At the beginning of 1986, that number had mushroomed to well over 10,000. Hundreds of newcomers are Joining our ranks every month.

Packet channels are becoming clogged to the point of unusability in many areas of the country. Networking is needed to help reduce congestion and improve the overall capability of the burgeoning Amateur packet radio community. The NNC, if adopted by the Amateur Packet community, may provide a solution for development and implementation of Amateur networking protocols.